ISSN 1991-1696

SAIEE

Africa Research Journal

Research Journal of the South African Institute of Electrical Engineers

Incorporating the SAIEE Transactions

www.saiee.org.za

March 2017
Volume 108 No. 1

SAIEE AFRICA RESEARCH JOURNAL

(SAIEE FOUNDED JUNE 1909 INCORPORATED DECEMBER 1909)
AN OFFICIAL JOURNAL OF THE INSTITUTE

ISSN 1991-1696

Published by
South African Institute of Electrical Engineers (Pty) Ltd, PO Box 751253, Gardenview, 2047
Tel. (27-11) 487-3003, Fax. (27-11) 487-3002,
E-mail: researchjournal@saiee.org.za

Additional reviewers are approached as necessary

ARTICLES SUBMITTED TO THE SAIEE AFRICA RESEARCH JOURNAL ARE FULLY PEER REVIEWED PRIOR TO ACCEPTANCE FOR PUBLICATION

The following organisations have listed SAIEE Africa Research Journal for abstraction purposes:

INSPEC (The Institution of Electrical Engineers, London); 'The Engineering Index' (Engineering Information Inc.)

VOL 108 No 1
March 2017

SAIEE Africa Research Journal

DESIGN AND OPTIMISATION OF A PCB EDDY CURRENT DISPLACEMENT SENSOR

A.J. Grobler* , **G. van Schoor†** and **E.O. Ranft***

* *School of Electrical, Electronic and Computer Engineering, North-West University, Potchefstroom, South Africa, e-mail: andre.grobler@nwu.ac.za*

† *Unit for Energy and Technology Systems, North-West University, Potchefstroom, South Africa.*

Abstract: Position sensing is one of the crucial parts of many systems, specifically in an active magnetic bearing. The position is used to control the magnetic forces within an active magnetic bearing to keep a rotor levitated. Sensors used in these systems must be very sensitive and are usually very expensive. In this paper a low cost printed circuit board position sensor is analysed. The sensor uses an excitation coil to establish a magnetic field. Four sensing coils are then used to measure the influence a conducting target has on the magnetic field to enable position sensing. The sensor's magnetic operation is analysed using finite element methods and very good correlation is found with measured results. The effects of the target material and the number of PCB layers are analysed. It is shown that a two layer sensor can produce acceptable sensitivity and linearity.

Key words: eddy current, displacement sensor, multiple layer PCB

1. INTRODUCTION

In active magnetic bearings (AMB) systems accurate position sensing of the levitated object, mostly a rotating rotor, is essential. Due to its impact both in terms of cost and reliability, position sensing in AMB systems is an important research topic. Two currently prominent approaches to determining the rotor position are self-sensing and dedicated non-contact sensors. In self sensing, the rotor position is approximated using the change in actuator inductance, caused by rotor movement [1, 2]. Dedicated position sensor technologies used in AMBs, include; optical, inductive, eddy current, Hall-effect and capacitive types [3]. AMB systems have very small airgaps between the rotor and stator, usually around 0.5 mm. The rotor can thus only move 0.25 mm in the radial direction before making contact with the backup bearings.

Eddy current sensors induce eddy currents in a conducting target and uses the change in magnetic field due to the eddy currents to measure various physical parameters. A single coil can be used as the excitation and measuring coil in which case the change in inductance is usually detected through the change in oscillation frequency of the excitation circuit. Sensing coils are not connected to the excitation coil and a change in induced voltage can be measured using analog to digital converters. These sensors are commonly used to measure lateral displacement [4], rotation [5] and axial displacement [6]. It is also used to detect defects in materials like PCBs [7] and is highly dependent on material properties [8]. These sensors have also been used in condition monitoring, for example measuring turbine rotor vibrations [9], [10]. Various applications require that flexible PCBs be used to reach in small spaces [11]. Vyroubal has developed transformer equivalent circuits for the probes [12] as well as improving the driving circuitry [13].

Philipp Bühler registered a patent in 2002 [14] for a device to measure a rotor position in multiple directions. In 2004, Larsonneur and Bühler presented a printed circuit board (PCB) sensor, based on the aforementioned patent, for measuring radial movement of the rotor in an AMB system [15]. This concept was also used to develop a sensor for high temperature AMBs, using thick-film manufacturing techniques [16]. Larsonneur and Bühler reported that modelling of the sensor should be explored further as "model predictions do not yet satisfyingly agree with measurement results" [15]. The contribution of this article is showing a two-dimensional finite element method (FEM) model can accurately predict the sensor's output for movement perpendicular to the sensing coil.

The probe of this sensor comprises an excitation coil and four sensing coils; all planar coils formed using PCB tracks. Figure 1(a) and (b) illustrate the sensor arrangement through a side and top view respectively. A high frequency sinusoidal current (1-10 MHz) is applied to the excitation coil, thus establishing a varying magnetic field around it. The four sensing coils are placed around the excitation coil, each covering about a quarter of the circumference of the target. Placing a conductive target inside the excitation coil causes eddy currents to flow in the target. When the target is moved relative to the probe, magnetic field coupling to the sensing coils will be influenced by the eddy currents flowing in the target. When the target is close to a sensing coil, the magnetic field coupling with the sensing coil will be decreased by the eddy currents. Similarly a larger magnetic field coupling with the sensing coil located far from the target will prevail.

As explained above, the target should be electrically conductive for an eddy current sensing principle to be used. The penetration depth (δ) of the magnetic fields can be calculated using

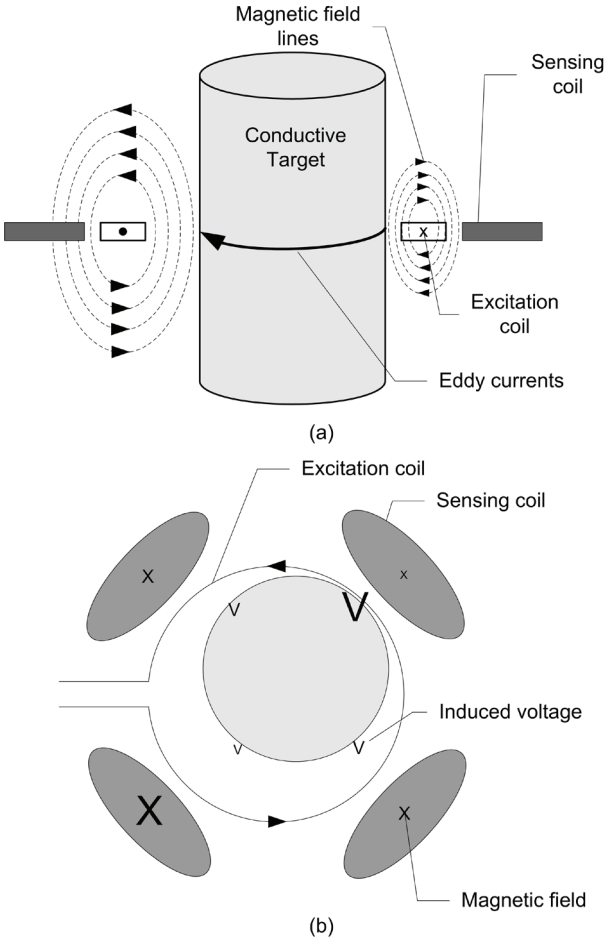


Figure 1: PCB eddy current displacement sensor: (a) Side view and (b) top view [15].

$$\delta = \sqrt{\frac{2}{2\pi f \mu \sigma}} \tag{1}$$

where f is the frequency of the excitation current, μ is the permeability and σ is the conductivity of the target. Aluminium is commonly used as target for eddy current sensors and has a calculated penetration depth of 58.5 µm if a 2 MHz signal is used. Stainless steel, for example SAE 304, is also widely used in AMB rotors since it has a high yield strength and does not influence the AMB's magnetic field as it is non-magnetic. The penetration depth of SAE 304 at 2 MHz is calculated as 302 µm. If a magnetic material is used as the target the penetration depth will be significantly smaller. Mild steel has a calculated penetration depth of less than 10 µm. In the AMB environment the position sensing is usaually done on a non-magnetic surface. As the position sensor's target on the rotor is placed very close to the AMB, a magnetic target will introduce hytesteresis losses if a heteropolar radial AMB is used.

This article presents a FEM model for a PCB sensor in Section 2. The model is verified using a purpose built test platform as discussed in Section 3. In Section 4 the optimal sensor configuration is analysed to deterimine the impact some paramenters has on performance.

2. MODELLING

Deriving an accurate model for the PCB sensor can help the designer understand the influence a certain parameter has on the operation and performance of the sensor. A model can be used to ensure specifications are met when designing a sensor. A model can perdict the behavior of the sensor in various conditions and operating modes.

The computational resources needed to solve a FEM model are influenced by the number of nodes in the model. If the three-dimensional reality has a symmetry axis, a two-dimensional approximation can be made without decreasing the accuracy of the model. Figure 2 shows the two-dimensional approximation of the PCB sensor. The excitation and sensing coils will be realised with tracks on a PCB as shown in the lower part of the figure. In an approximation in the upper part of Figure 2, the excitation coils are modeled as a rectangle with the same dimensions of the tracks and half the current density, thus incorperating the voids between the tracks. The sensing coil is approximated with a line, since only the magnetic flux passing through this line will be used further to calculate the induced voltage. This model is implemented in COMSOL Multiphysics® using the axial symmetry Quasi-Statics Azimuthal Currents application mode.

The sensing coils' voltages are the main model output. A coil voltage (e) can be determined using Faraday's law, shown in (2), if the change in magnetic flux ($\Delta\Phi$) through the sensing coil, number of turns on the coil (N) and period of the excitation current (Δt), are known.

$$e = N\frac{d\Phi}{dt} \simeq N\frac{\Delta\Phi}{\Delta t} \tag{2}$$

The magnetic flux can be determined using (3), where B is the magnetic field density and A the sensing coil area.

$$\Phi = \int BdA \tag{3}$$

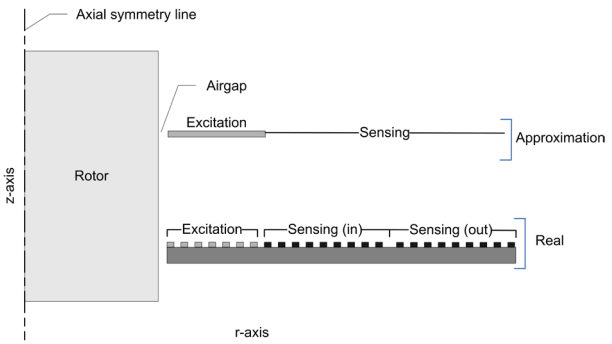


Figure 2: FEM model assumptions

Sensitivity and linearity are two of the performance parameters used when optimising the sensor. Sensitivity (S) is the ratio of voltage change (ΔV) and displacement (Δx), see (4). Linearity gives an indication of how close the calibration curve fits a straight line. The maximum deviation above and below the straight line, V_{MT} and V_{MB}, and the total displacement (Δx), are used to determine linearity, as given by (5).

$$S(V/m) = \frac{\Delta V}{\Delta x} \tag{4}$$

$$\text{Linearity } (\%) = \frac{V_{MT} - V_{MB}}{\Delta x} \times 100 \tag{5}$$

Figure 3 shows the magnetic fields established by the excitation coil and passing through the sensing coils. The magnetic fields passing through the target induces eddy currents in the target. Figure 4 shows the modelled peak voltage induced in a sensing coil when a target is moved between 0.25 mm and 0.75 mm from the PCB. The results for three different materials (SAE 304 stainless steel, copper and aluminium) are shown. The conductance (σ) and permeability (μ) of the target influences the eddy currents flowing in the target and thus the amplitude of the voltage induced in the sensing coil. Copper is the most conductive, thus a smaller voltage is induced when compared to stainless steel that is less conductive.

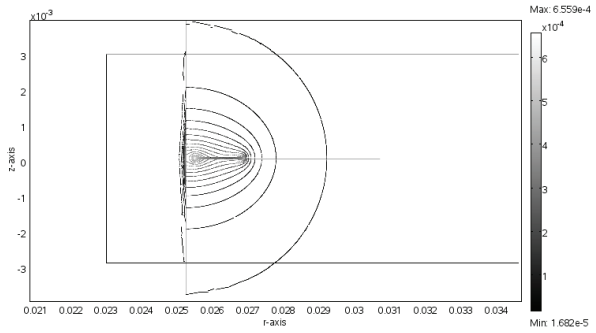


Figure 3: Simulated magnetic fields established by the excitation coil

The simulation results shown in Figure 4 support the sensor operation described previously. There is a sufficient change in voltage to warrant manufacturing a prototype sensor. This prototype will be used to verify the model presented in this section.

3. MODEL VERIFICATION

3.1 *Evaluation platform*

To verify the FEM model, a sensor was designed using the model and constructed using standard PCB manufacturing techniques. An evaluation platform was also developed as is shown in Figure 5. The reference position was measured by two eddyNCDT 3701 sensors

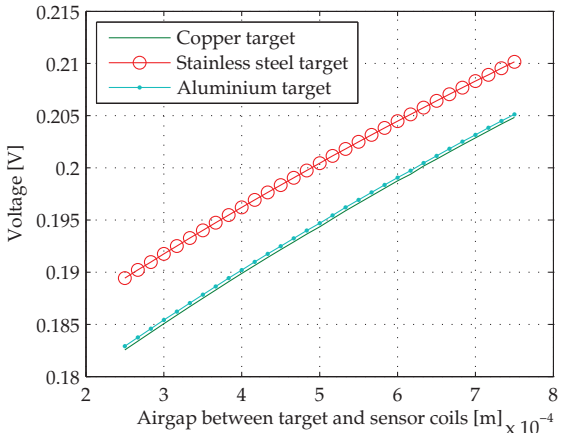


Figure 4: Simulated sensing coil voltage for different materials when changing the airgap.

from MICRO-EPSILON® on an aluminium target. These sensors can measure on any conductive material but were calibrated on aluminium. These sensors have a measuring range of 1 mm, linearity of 6 % full scale output (FSO), $<$ 0.001 % FSO repeatability, $<$ 0.000033 % FSO static resolution and $<$ 0.00016 % FSO dynamic resolution. In the test setup, movement is always parallel with a coil pair (e.g. coils 1 and 3) and perpendicular with the other coil pair (e.g. coils 2 and 4).

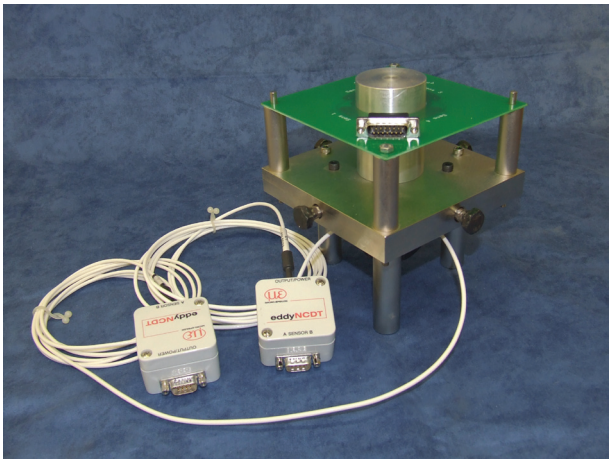


Figure 5: Evaluation platform.

3.2 *Comparing simulation and measured results*

This section compares the simulation results to the measured results. The voltage on a sensing coil was recoded for 10 µs (or 20 cycles), sampled at 2.5 GHz using the LeCroy® WaveRunner® 6030A digital oscilloscope. Ten data sets were recorded and the amplitude of the fundamental frequency determined using fast Fourier transform in MATLAB. The median of these 10 values represents a data point, referred to as measured voltage.

Figures 6 and 7 show the voltage measured on the four sensing coils of the single layer sensor when moving the

aluminium target from sensing coil 4 towards sensing coil 2 as well as moving from sensing coil 1 towards sensing coil 3. This movement causes an increase in the airgap between sensing coil 4 (1) and the target. As a result the voltage measured on sensing coil 4 (1) and 2 (3) decreases and increases, respectively. Due to the symmetry in the model, the model results for sensing coil 2 (3) have the same but negative gradient and the values but will decrease as the airgap increase, labled "Simulation decrease" in Figure 6. The sensing coils are numbered 1 - 4 in a clockwise rotation, starting at the coil just right of the connector.

There is a dc offset in all measurements compared to the model results. This can be attributed to voltage induced in the connection track of the sensing coils by the excitation coil magnetic field. The voltages measured across sensing coils remain constant when the target does not move relative to these coils. Again there is some dc offset and the voltages measured on sensing coils 3 and 2 are larger as these have longer connection tracks.

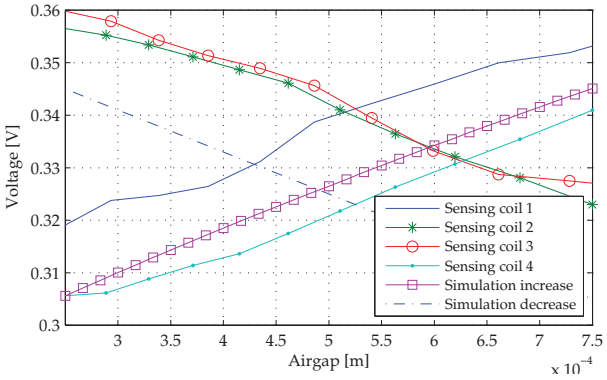


Figure 6: Induced voltage on sensing coils 1 to 4 including simulation results when moving in the direction of the coils (1 layer sensor).

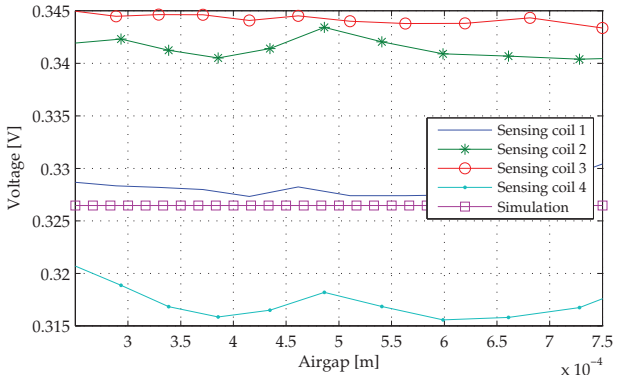


Figure 7: Induced voltage on sensing coils 1 to 4 including simulation results when moving perpendicular to the coils (1 layer sensor).

Differential measurements of opposite coils will be used when implementing the sensor as this will reduce the influence of common mode effects like temperature and magnetic interference. The sensitivity is also doubled. Differential measurements were taken for the 2-layer sensor, moving an aluminium target between sensing coil 1 and 3. Figure 8 shows the differential results. Sensing coils 1 and 3 results closely agree with that predicted by the model.

Table 1 compares the sensitivity results for 2 different target materials when the single-layer sensor is used. The results when using aluminium (Al) and stainless steel (Ss) targets show good correlation between modelled and measured results.

Table 1: Sensitivity comparison

Target material	Sensing coil no.	Model [V/m]	Measured [V/m]	Difference [%]
Al	1	158	155.41	1.63
Al	2	158	140.12	11.31
Al	3	158	151.49	4.12
Al	4	158	147.85	6.42
Ss	2	148.62	138.35	6.91
Ss	4	148.62	148.37	0.17

Table 2 shows the results for the double-layer sensor when an aluminium target is used. The results of the two sensing coil pairs (1&3, 2&4) are not the same. Sensing coils 1 and 3 measured results correlate well with the modelled results. Sensing coils 2 and 4 results do not show good correlation with the model. The next section will discuss a possible cause for the difference in results.

Table 2: Sensitivity comparison: Double-layer with Aluminium target.

Sensing coil no.	Model [V/m]	Measured [V/m]	Deviation [%]
1	335.25	338.50	0.96
2	335.25	253.85	24.28
3	335.25	335.73	0.14
4	335.25	264.16	21.2

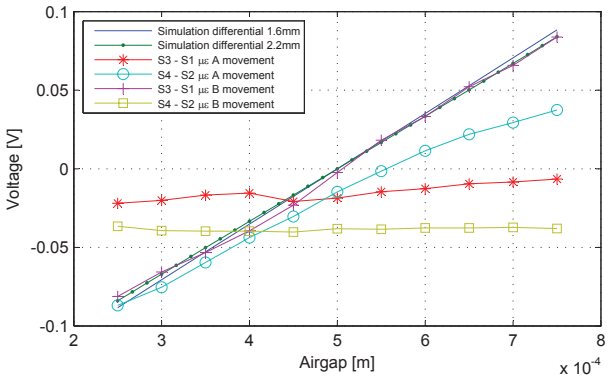


Figure 8: 2-layer sensor: differential results for an aluminium target.

3.3 *Oscillator circuit drift*

The excitation current was created using a voltage-to-current circuit and a bench signal generator (EZ® Digital FG7020A), together called the oscillator circuit. In this section the change of the measured sensing coil voltage over time is investigated. Figure 9 shows the rms voltage measured on a sensing coil against a number of measurements. The target is not moved and no changes are made to the test setup. The voltage was measured using a LeCroy® WaveRunner® 6030A digital oscilloscope. Measurements 1 to 24 are taken after the oscillator circuit operated for a long time ($>$ 7 hours), measurements 25 to 53 were taken 10 minutes after switching on the oscillator circuit and measurements 54 to 78 are taken 1 hour after switching on the oscillator circuit. At the start of each measuring series the oscillator voltage is adjusted to ensure a 100 mA rms current is flowing in the excitation coil. Each of the measurement series is taken over a 6 minute time frame in 15 second intervals.

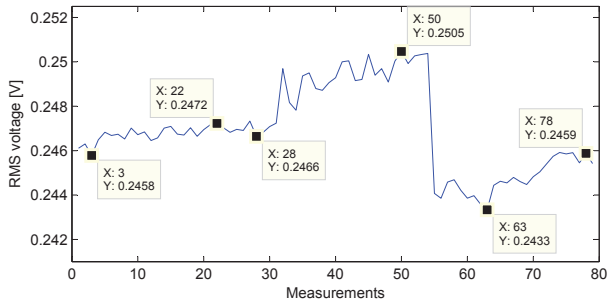


Figure 9: Sensing coil 2 voltage showing oscillator drift.

When the circuit was active for a long time (measurements 1 to 24) there is not a significant change in the voltage. But when considering the large change when just switching on the circuit and when adjusting as at measurement 54, it is clear that the oscillator circuit has a significant influence on the measurements. Considering the small change in voltage (around 40 mV for the single layer) when moving the target through the whole range, the measurements shown in Figure 9 could easily cause a 10 % error as seen in Table 1. The large deviation in sensing coils 2 and 4 seen in Table 2 when moving in the sensing coil 2 direction could thus be caused by oscillator circuit drift.

Note that there are also other differences when comparing the experimental setup to the simulation results. Sensing coils 2 and 3 have longer tracks from the connecter to the coil that sensing coils 1 and 4. It was found that the difference can be as big as 100 mV, thus accounting for the dc offsets seen in Figures 6 and 7. But these differences remained the same, regardless of the target movement and would thus not influence the sensor's sensitivity.

4. OPTIMISATION CONSIDERATIONS

This section presents some of the considerations to design an optimal sensor using the model presented in the previous section. Table 3 lists the optimisation criteria and variables that can be modified to optimise the sensor performance as well as some of the paramenters assumed to be constant.

Linearity is the least crucial performance parameter since the position signal can be linearised by applying a function fit to the calibration curve. Figure 10 shows the modelled linearity (in percentage of full scale output (FSO) of a single sensor when varying the number of excitation coil windings (n_{exc}) and the number of sensing coil windings (n_{sens}). An exponential decrease in linearity can be seen when increasing either variables. All of the combinations where $n_{exc} > 5$ and $n_{sens} > 5$ have a linearity smaller than 0.3 % FSO, an acceptable value for the sensor.

The modelled sensitivity for different combinations of n_{exc} and n_{sens} are shown in Figure 11. Increasing n_{sens} causes an increase in sensitivity. When increasing n_{exc}, sensitivity also increases but reaches a turning point, clearly seen when $n_{sens} = 15$ and $n_{exc} = 1 \rightarrow 15$. According to this figure, n_{sens} should be as large as possible and n_{exc} should be chosen on a turning point, when designing an optimal sensor. More insight can be gained by considering the gradient of the sensitivity when varying n_{sens} and n_{exc}, as shown in Figure 12. From this figure it is clear that for a certain n_{sens}, a maximum gradient of sensitivity can be found by varying n_{exc}.

The number of layers the PCB sensor is implemented on can also be varied to optimise the sensor's sensitivity and signal level. A high signal level is beneficial when the noise effects between the sensor and demodulation circuitry must be minimised. The conductors connecting the sensing coils and the demodulation circuitry will, in some cases, be long and routed in noisy environments. Figure 13 shows the voltage induced on a sensing coil

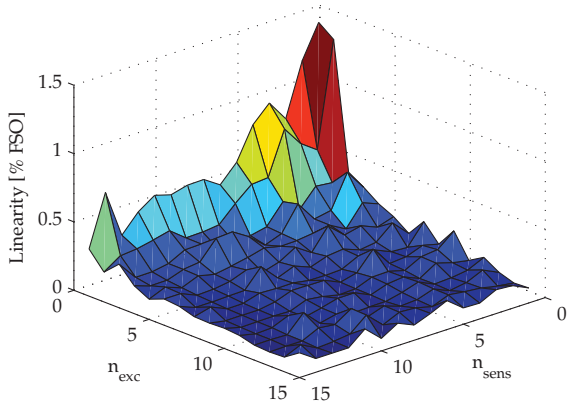


Figure 10: Modelled linearity for excitation coil windings ($n_{exc} = 1 \rightarrow 15$) and sensing coil windings ($n_{sens} = 1 \rightarrow 15$).

Table 3: Optimisation criteria and variables

Optimisation criteria	
Linearity, Sensitivity, Signal level, Cost	
Variables	
Number of sensing coil windings	n_{sens}
Number of excitation coil windings	n_{exc}
Number of PCB copper layers	
Track width and spacing	
Insulating material thickness	
Target material	
Constants	**Values**
Excitation frequency	2 MHz
Excitation current	100 mA
Excitation voltage	$\pm 15 V_{dc}$
Target size diameter	50 mm
Minimum airgap	0.25 mm
Movement range	0.5 mm
Track height	0.035 mm

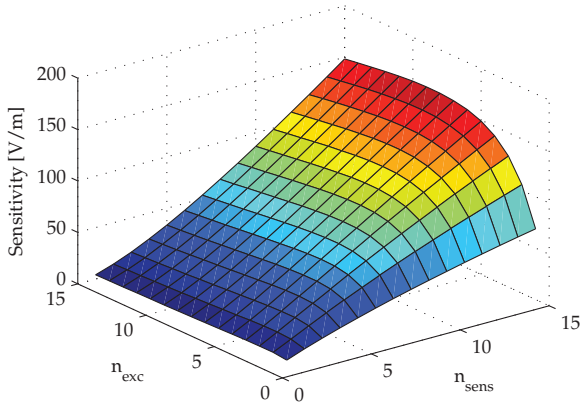


Figure 11: Modelled sensitivity for no. of excitation coil windings ($n_{exc} = 1 \rightarrow 15$) and no. of sensing coil windings ($n_{sens} = 1 \rightarrow 15$).

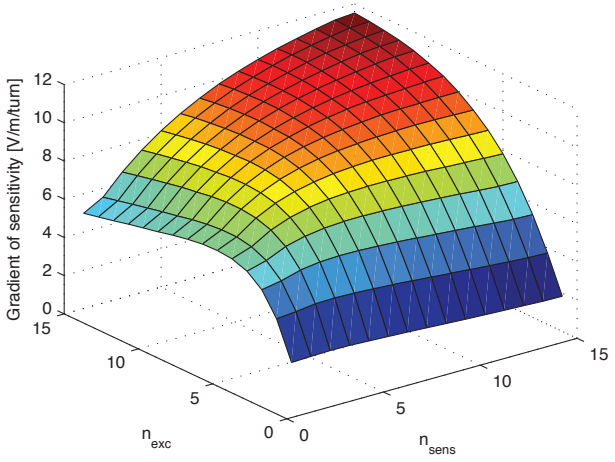


Figure 12: Modelled gradient of sensitivity for excitation coil windings ($n_{exc} = 1 \rightarrow 15$) and sensing coil windings ($n_{sens} = 1 \rightarrow 15$).

when varying the airgap, for a single-, double- and five-layer sensor configuration. The signal level and sensitivity increase with an increase in number of PCB layers. Unfortunately, the cost of manufacturing the PCB also increases when the number of PCB layers increase. A five-layer sensor costs ten times more to manufacture than a single-layer sensor. It was found that a double-layer sensor is the best option when considering cost and sensitivity.

The conductive layers of a PCB are placed on an insulating material (fr4). The effect of varying this thickness must also be investigated. Figure 14 shows the induced voltage vs. airgap for four fr4 thicknesses: 0.1, 0.5, 1.6 and 2.2 mm. The standard fr4 thickness is 1.6 mm, thus this figure represents the whole range of commonly found fr4 thicknesses. A small improvement in sensitivity and signal level is found when using a thinner insulation layer. This can be attributed to an increase in the magnetic coupling between the excitation and sensing coils located on the different layers. A thinner insulation material is more fragile and expensive to manufacture, and the performance improvement is not significant when compared to other variables.

The influence of changing the copper track width and spacing is the final variables explored in this article. Figure 15 shows the induced sensing coil voltage when adjusting the airgap, for different combinations of excitation and sensing coil's track spacing and width. The signal level is significantly higher when a narrower excitation coil track width and spacing is used. In this situation, the same magnetic flux is generated by a physical smaller coil thus more of the magnetic flux couples to the sensing coil, inducing an larger voltage in it. The sensing coil's track spacing and width does not significantly influence the signal level.

Sensitivity is increased when using a narrower excitation coil track and spacing. In this situation, the sensing coils are located close to the target, thus more sensitive for target movement. The sensitivity is marginally increased when increasing the sensor coil's track width and spacing.

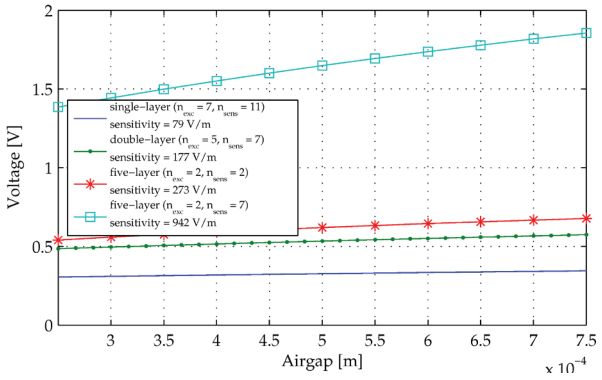


Figure 13: Induced sensing coil voltage vs. displacement for 1, 2 and 5 layer sensors.

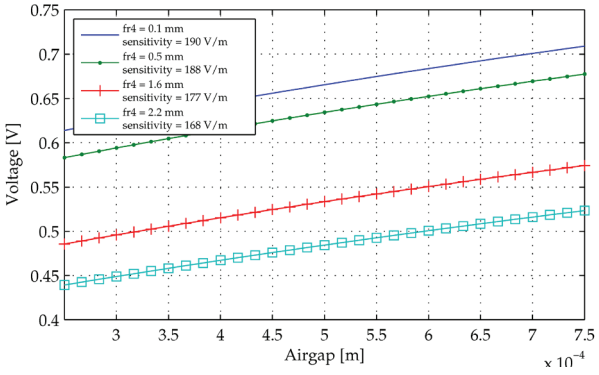


Figure 14: Modelled induced sensing coil voltage vs. displacement for different insulation material thicknesses.

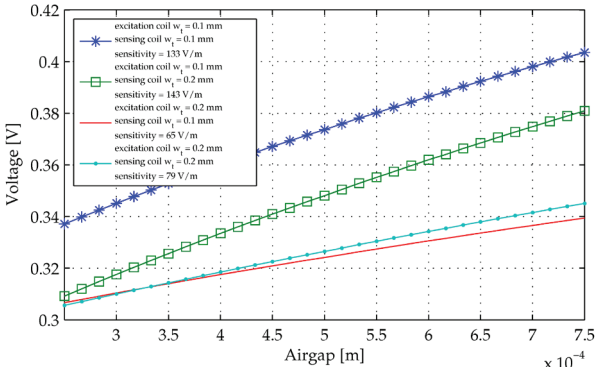


Figure 15: Modelled induced sensing coil voltage vs. displacement for different track spacing and track width.

5. CONCLUSION

This article presented a low cost, eddy current displacement sensor. The sensor unit can be produced very cheaply by using PCBs to realise the sensor coils. The sensor is designed to use in AMBs and was tested on a representative rotor diameter. The number of excitation and sensing coil turns that will result in an optimal sensitivity and linearity have been identified using FEM simulations. The FEM model was verified using an evaluation platform where MICRO-EPSILON® eddy current sensors were used as reference. Aluminium, stainless steel and mild steel targets were used and good correlation achieved for the first two.

The use of multi-layer PCBs was also investigated. Increasing the number of layers led to a significant increase in sensitivity. This came at a significant increase in manufacturing cost. It is thus proposed that a standard thickness FR4, double layer PCB be used with 0.2 mm tracks and spacing be used. The sensor can then be manufactured for less than 2 % of the cost of eddy current sensors usually used in AMB systems. Note that the drive electronics, amplification and signal processing required to give an position output have not been included in the cost as these components are still being developed.

Future work will include futher modelling and characterisation to assess the viability of the concept. This includes 3D FEM modelling to establish the linearity of the final sensing results in the 2 principal directions. This will also involve signal processing using all four sensing signals. Finally the electromagnetic compatibility of the sensor in an actual AMB system with all possible electromagnetic disturbances should be investigated.

REFERENCES

[1] E. O. Ranft, G. van Schoor, and C. P. du Rand, “An integrated self-sensing approach for active magnetic bearings,” *SAIEE African Research Journal*, vol. 4, pp. 90 – 97, 2011.

[2] G. van Schoor, A. Niemann, and C. du Rand, “Evaluation of demodulation algorithms for robust self-sensing active magnetic bearings,” *Sensors and Actuators A: Physical*, vol. 189, no. 0, pp. 441 – 450, 2013.

[3] G. Schweitzer, H. Bleuler, and A. Traxler, *Active magnetic bearings : Basics, Properties and Applications of Active magnetic bearings*. Zurich: Authors Working Group, 2003.

[4] L. Weiwen, Z. Hui, and Q. Hongli, “Research on novel grating eddy-current absolute-position sensor,” *Instrumentation and Measurement, IEEE Transactions on*, vol. 58, no. 10, pp. 3678–3683, Oct 2009.

[5] A. Wogersien, S. Samson, J. Guttler, S. Beiftner, and S. Biittgenbach, “Novel inductive eddy current sensor for angle measurement,” in *Sensors, 2003. Proceedings of IEEE*, vol. 1, Oct 2003, pp. 236–241 Vol.1.

[6] P. Wang, Z. Fu, and T. Ding, “A frameless eddy current sensor for cryogenic displacement measurement,” *Sensors and Actuators A: Physical*, vol. 159, no. 1, pp. 7 – 11, 2010.

[7] K. Chomsuwan, S. Yamada, and M. Iwahara, “Bare PCB inspection system with SV-GMR sensor eddy-current testing probe,” *Sensors Journal, IEEE*, vol. 7, no. 5, pp. 890–896, May 2007.

[8] G. Y. Tian, Z. X. Zhao, and R. W. Baines, “The research of inhomogeneity in eddy current sensor,” *Sensors and Actuators*, vol. A 69, pp. 148–151, 1998.

[9] J. Wilde and Y. Lai, “Design optimization of an eddy current sensor using the finite-elements method,” *Microelectronics Reliability*, vol. 43, no. 3, pp. 345 – 349, 2003.

[10] M. Tsutomu, G. Sho, D. Kenta, K. Yoshinori, A. Yuichi, E. Shigemi, and S. Hiroki, “Method for identifying type of eddy-current displacement sensor,” *Magnetics, IEEE Transactions on*, vol. 47, no. 10, pp. 3554–3557, Oct 2011.

[11] X. Chen and T. Ding, "Flexible eddy current sensor array for proximity sensing," *Sensors and Actuators A: Physical*, vol. 135, no. 1, pp. 126 – 130, 2007.

[12] D. Vyroubal, "Impedance of the eddy-current displacement probe: The transformer model," *IEEE Transactions on instrumentation and measurement*, vol. 53, no. 2, pp. 384–391, April 2004.

[13] ——, "Eddy-current displacement transducer with extended linear range and automatic tuning," *Instrumentation and Measurement, IEEE Transactions on*, vol. 58, no. 9, pp. 3221–3231, Sept 2009.

[14] P. Bühler, "Device for cantact-less measurement of distances in multiple directions," Europe Patent 1 422 492, May 26, 2004.

[15] R. Larsonneur and P. Bühler, "New radial sensor for active magnetic bearings," in *International Symposium on Magnetic Bearings*, no. 9, Lexington, Kentucky, USA, August 2004.

[16] L. Burdet, T. Maeder, R. Siegwart, P. Bühler, and B. Aeschlimann, "Thick-film radial position sensor for high temperature active magnetic bearings," in *Symposium on Magnetic Bearings*, no. 10, Marigny, Switzerland, August 2006.

A RANKING METHOD FOR RATING THE PERFORMANCES OF PERMUTATION CODES

K. Ogunyanda* **and T.G. Swart***

* *Department of Electrical and Electronic Engineering Science, University of Johannesburg, Auckland Park, 2006, South Africa. Email: ogunyanda@gmail.com and tgswart@uj.ac.za*

Abstract: Minimum Hamming distance, d_m, has been widely used as the yardstick for the performance of permutation codes (PCs). However, a number of PCs with the same d_m and cardinality can have different performances, even if they have the same distance optimality. Since PC is a robust channel coding scheme in power line communications applications, we present a simple and fast ranking method that predicts the relative performance of PCs, by using the information extracted from their Hamming distance distributions. This tool is useful for selecting an efficient PC codebook out of a number of similar ones.

Key words: Channel coding, Hamming distance distribution, Permutation coding, Power line communications, Ranking method.

1 INTRODUCTION

Power line communications (PLC), which involves information transmission through the existing power network, is now a popular technology that may be used for home internet access, data distribution, networking, smart metering and electric vehicle-to-charging stations. The major setback of this technology is the performance degradation posed by the various noise types present in the communication channel (i.e. power line). These noise types include background noise, impulsive noise and narrowband interference [1, 2]. These noise types are inherent in the channel, because the main purpose of the power line network is not for communication applications. In order to make the channel conducive for communications, it may be helpful to use higher transmission power or distortion-free frequencies in the communication system. There are, however PLC communication standards that enforce constraints on the range of power and frequencies that are useable [3–5]. As such, in order to achieve effective PLC systems, a robust channel coding scheme is a crucial component to consider.

The channel coding scheme of interest in this work is permutation coding (PC). This is motivated based on the foundational work on PCs reported by Vinck, who was the first to suggest its usage for PLC applications [1]. According to Vinck, PCs in combination with MFSK are capable of handling the types of noise associated with narrowband PLC channels. This then gave inspiration for more research works on PCs, some of which are reported in [6–16].

There have been some approaches to the generation of PC codebooks with different minimum Hamming distances and cardinalities. The term d_m refers to the minimum Hamming distance between any two distinct codewords in a codebook, $\mathcal{C}$, while $|\mathcal{C}|$ is the cardinality, which is the total number of possible codewords in the codebook. However, how one selects the best codebook out of a number of competitive PC codebooks with similar characteristics, is a challenging problem that we have attempted to solve in this study. The quality of a communication system can be greatly impaired if a poor code design is used.

In coding, d_m is usually used to determine the strength of a code in handling errors. According to [2], a PC is able to detect t symbol errors provided that:

$$t \leq (d_m - 1). \tag{1}$$

Moreover, in terms of error correcting capability, a PC is able to correct $t/2$ number of errors. However, apart from the d_m in a given codebook, other distances greater than d_m also feature, when the distance relationships between every distinct codeword are computed. All of these distances have a cummulative contribution in the performance of any given codebook. This notion was used by Viterbi in [19], when he demonstrated that various possible distances, resulting from every remerging path in the trellis-code representation of a convolutional code, contribute to its error probability. A similar approach was used in [20–22] to determine the distance spectrum used for comparing the performances of convolutional codes with similar constraint lengths and decoding complexities. We thus employ a similar approach in the ranking method presented in this study. However, instead of using it in the context of convolutional codes, it is used in the context of non-binary PC schemes. Also, Hamming distance distribution is what we have used in this study, instead of the distance spectrum used in convolutional code, which is a binary code. As such, this study is centered on determining the cumulative effects of all the possible distances, including d_m, on the error detecting capability of any given PC.

Other work done in repect of PCs' performance tools include the one reported in [23], where a probabilistic approach was used to determine PC decoders' performances. However, this is not related to the work presented here, in

that our approach is not decoder-dependent, as opposed to the work in [23], which is based on the type of decoding algorithm used in the design.

In addition, instead of using cardinality and Hamming weight distribution, Hamming distance distribution (HDD), which takes into consideration the contribution of every possible distance, is employed in our work. The reason for this is discussed later in this paper. To the best of our knowledge, this is the first time a method such as this is employed for PCs.

It is however worth noting that the ranking method presented here is only evaluated based on combined background noise (modeled as AWGN) and impulsive noise channel conditions. As such, a representation of AWGN+IN channel model is involved in this work. In order to study the performance of data transmission over a PLC channel, the authors in [24] used Middleton's model to model the transmission channel using a binary symmetric channel, whose transmission error probability ε is dependent on the impulsive noise variance. In our proposed ranking method, we represent the channel model as a composite channel, comprising of the modulator, demodulator and the PLC channel. This composite setup is appropriate, in order to be able to analyse channel codings [25]. The ε of this channel setup is derived from Middleton's noise model for impulsive noise.

Our contribution in this work therefore further promotes the use of PCs in PLC-related applications, by providing a good ranking tool that can be used to rate the performances of PC schemes of similar characteristics, without the need to perform performance simulations. Having to perform performance simulations for a multitude of codebooks, where each simulation could take a considerable time to complete, would mean that the process of choosing the best codebook will be extremely time consuming. In practical terms, this tool can be handy, when the best codebook is to be chosen out of a number of competitive codebooks. In [17] and [18], various PC codebooks of the same $|\mathcal{C}|$ and d_m were presented which had the same distance optimality, but their performances are seen to be slightly different when simulated. The method proposed here is therefore able to determine the best PC codebook in such situations. Hence, this work can be viewed as an extension of the work reported in [17] and [18].

We briefly describe what PC entails in Section 2. Section 3 gives a brief background to the HDD of a codebook, which is then used to propose the PC ranking method in Section 4. In Section 5, we present the HDDs of some known PCs and use the proposed method to analyse and predict their performances. Some simulation results are presented in Section 6 to validate the analysis performed in Section 5, after which a concluding note is given in Section 7.

2 INTRODUCTION TO PERMUTATION CODING

As stated in [9], a PC mapping maps binary data sequences to codewords of non-binary permutation sequences. A PC codebook is usually denoted as $\mathcal{C}(n,M,\eta)$, where n is the number of bits being mapped onto M symbols, while η determines the mapping type. Each codeword is of length M, and its symbols are chosen from $\{0,1,\ldots,M-1\}$. An example of a PC, with codeword length $M=4$, where $n=2$ bits are mapped to the PC symbols [9], is:

$$\{00,01,10,11\} \rightarrow \{2130,2103,3120,0213\}. \quad (2)$$

Another example with $M=4$ and $n=4$ is [18]:

$$\begin{Bmatrix} 0000,0001,0010,0011, \\ 0100,0101,0110,0111, \\ 1000,1001,1010,1011, \\ 1100,1101,1110,1111 \end{Bmatrix} \rightarrow \begin{Bmatrix} 1230,1203,1320,1302, \\ 2130,2103,3120,3102, \\ 0231,0213,0321,0312, \\ 2031,2013,3021,3012 \end{Bmatrix}. \quad (3)$$

If the distances between the binary and permutation sequences are compared, three types of PC mappings can be defined, namely distance-conserving mappings (DCMs), distance-increasing mappings (DIMs) and distance-reducing mappings (DRMs). For instance, the binary sequences in (2) have $d_m = 1$, while their corresponding permutation sequences have $d_m = 2$. With this, $\eta = 1$. Hence, such a PC mapping is a DIM. By definition, a DIM ensures that the distances of the permutation sequences have some increase above the those of the binary sequences; a DCM ensures that the distances of the binary sequences are at least maintained in their corresponding permutation sequences; and a DRM ensures a controlled distance loss between distances. These three mapping types are collectively referred to as distance-preserving mappings [17, 26].

A number of PC mapping and decoding algorithms are available in the literature. However, since we are only focusing on analysing PCs' relative performance, the simulations done in this work have considered the simple PC mapping and decoding algorithm presented in [9]. Therein, information bits are grouped into n bits, and these grouped bits are in turn mapped to corresponding codewords of length M, based on the grouped bit sequences. On the decoding side, a codeword having the closest Hamming distance to the received codeword is selected as the decoded codeword.

3 HAMMING DISTANCE DISTRIBUTION

We define HDD as the amount of contribution each possible Hamming distance has in the performance of a given PC codebook. Let Hamming distance k be represented by d_k. Given a codebook $\mathcal{C}$, with M and d_m, all the possible distances d_k in $\mathcal{C}$ are given by:

$$k \in \{0,1,\ldots,M\}. \quad (4)$$

If the minimum distance is d_m, (4) therefore reduces to

$$k \in \{d_m, d_m+1,\ldots,d_M\}, \quad (5)$$

If the distance relationship between every distinct

codeword in $\mathcal{C}$ is computed, a $|\mathcal{C}| \times |\mathcal{C}|$ dimensional distance matrix $\mathbf{E}$ is generated. This matrix $\mathbf{E}$ consists of elements $e_{i,j}$ that represent the distance between every pair of distinct codewords x_i and x_j in the codebook, where $i, j = 1, 2, \ldots, |\mathcal{C}|$ and is defined as:

$$\mathbf{E} = \begin{array}{c} \\ x_1 \\ x_2 \\ \cdot \\ \cdot \\ \cdot \\ x_{|\mathcal{C}|} \end{array} \begin{array}{c} \begin{array}{ccccc} x_1 & x_2 & . & . & . & x_{|\mathcal{C}|} \end{array} \\ \begin{pmatrix} e_{1,1} & e_{1,2} & . & . & . & e_{1,|\mathcal{C}|} \\ e_{2,1} & e_{2,2} & . & . & . & e_{2,|\mathcal{C}|} \\ . & . & . & . & & . \\ . & . & . & . & & . \\ . & . & . & & . & . \\ e_{|\mathcal{C}|,1} & e_{|\mathcal{C}|,2} & . & . & . & e_{|\mathcal{C}|,|\mathcal{C}|} \end{pmatrix} \end{array}, \quad (6)$$

where $e_{i,j} = 0$, for $i = j$.

The total number of occurrences of each d_k can then be determined from the elements in matrix $\mathbf{E}$. For instance, the distance matrix for the codebook in (2) is given by:

$$\mathbf{E} = \begin{array}{c} \\ 2130 \\ 2103 \\ 3120 \\ 0213 \end{array} \begin{array}{c} \begin{array}{cccc} 2130 & 2103 & 3120 & 0213 \end{array} \\ \begin{pmatrix} 0 & 2 & 2 & 4 \\ 2 & 0 & 3 & 3 \\ 2 & 3 & 0 & 4 \\ 4 & 3 & 4 & 0 \end{pmatrix} \end{array}. \quad (7)$$

Let δ_k denote the number of times that d_k appears in the distance matrix. We can then express the HDD, Δ, of all the possible d_k as

$$\begin{aligned} &\Delta = \{\delta_1, \ldots, \delta_{m-1}, \delta_m, \delta_{m+1}, \ldots, \delta_{M-1}, \delta_M\}, \\ &\text{with } \delta_1, \ldots, \delta_{m-1} = 0. \end{aligned} \quad (8)$$

Using a probabilistic approach, the contribution of each d_k, given its δ_k, is given by:

$$P_k = \frac{\delta_k}{\sum_{k=m}^{M} \delta_k}, \quad m \leq k \leq M. \quad (9)$$

To illustrate this, the HDD and distance probabilities of the example codebook given in (3) are respectively given by:

$$\Delta = \{0, 64, 64, 112\}, \quad (10)$$

and

$$P_2 = P_3 = 0.2667 \text{ and } P_4 = 0.4667. \quad (11)$$

According to (11), it is clear that the codebook's performance mainly depends on d_4, since it has the greatest probability. The significance of the δ_k values (i.e., the HDD) in determining the strength of a PC can be understood by considering Viterbi's findings in [19]. In the trellis diagram of a convolutional code, any arbitrary path leading to a given node is associated with a distance, which is computed by determining the bitwise differences between the code sequences along such a path and the expected code sequence. In order to detect the optimum path, all the distance information, which are dependent on the channel transition probability, need to be computed [19].

Similar to convolutional codes where numerous different codes, with varying performance, can be obtained for the same parameters, various mappings from binary sequences to permutation sequences can be obtained, all having the same d_m and satisfying the distance preserving property. Thus a method was needed to determine which of these mappings would perform the best. The work in [17] and [18] addressed this by introducing the concept of distance optimality derived from distance matrix $\mathbf{E}$ like the one defined in (6). By denoting the sum of all distances in matrix $\mathbf{E}$ by $|\mathbf{E}|$, a PC is considered distance optimal if $|\mathbf{E}|$ is maximised. It was shown that an upper bound on $|\mathbf{E}|$ exists, and that any PC codebook attaining the bound would perform better than those that do not.

This clearly showed that all the distance contributions affect the performance of a given PC codebook. However, this approach is unable to distinguish between some codebooks with the same $|\mathcal{C}|$, d_m and maximised $|\mathbf{E}|$. Hence, we investigate the proposed PC ranking method that goes further in analysing the HDD, to enable us to distinguish between such codebooks.

In HDD, the diagonal elements of $\mathbf{E}$ is not considered, because this would amount to comparing a codeword with itself. Hamming weight distribution on the other hand, is the number of codewords with Hamming distance k from an all 0's reference codeword. This however holds for binary codes. For non-binary codes such as PCs, a reference origin codeword, which may or may not be in $\mathcal{C}$, is compared with each codeword, in order to determine the weight distribution [23]. One could state that HDD and weight distribution are the same, if the comparison is done with reference to an origin codeword. However, this is only valid for a linear code. Since PC is a non-linear code, to get accurate results every distinct codeword must be compared with all other codewords.

4 RANKING METHOD

In the context of this work, the term *ranking* refers to the order of performances of a given set of codewords, when being compared. The ranking method proposed in this study entails using the HDD discussed above to determine the probability of undetected symbol errors of a given codebook $\mathcal{C}$. Since the PCs considered in this study are non-binary codes, this necessitates the use of non-binary modulation, such as phase shift keying (PSK) modulation. In order to evaluate the error probability of a PC system using such modulations, we employ the composite channel setup in Fig. 1 as the transmission channel.

The PLC channel block is a combiation of impulsive noise and additive white Gaussian noise (AWGN). Since the

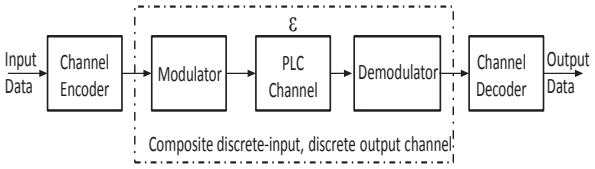


Figure 1: Channel model for ranking method.

modulator employs non-binary waveforms and the detector makes hard decisions, we can say that the composite channel has a discrete-time non-binary input sequence $X = \{0, 1, \ldots, M_{\mathrm{DP}} - 1\}$, where M_{DP} is a modulation order whose value is a power of 2, and a discrete-time non-binary output sequence. Each input symbol has a probability $1/M_{\mathrm{DP}}$ of being received at the output. The probability of receiving an incorrect symbol is $\xi = \varepsilon/(M_{\mathrm{DP}} - 1)$, while $(1 - \varepsilon)$ is the probability of correctly receiving a symbol at the detector's output, where ε is the transmission error probability.

If φ and α respectively denote a modulated and a demodulated symbol from the system, where $\varphi \in (0, 1, \ldots, M-1)$ and $\alpha \in (0, 1, \ldots, M_{\mathrm{DP}} - 1)$, the following expression therefore holds, based on the above composite channel setup:

$$P(Y = \alpha | X = \varphi) = \begin{cases} 1 - \varepsilon, & \text{if } \varphi = \alpha, \\ \xi, & \text{if } \varphi \neq \alpha. \end{cases} \tag{12}$$

Also, as stated in (1), a PC has a symbol error detecting capability of $(d_m - 1)$, which can be generalised for each d_k as

$$t_k = (d_k - 1) = (k - 1). \tag{13}$$

Since each d_k has its number of appearances δ_k, the probability of a PC detecting t_k number of errors is dependent on the value of δ_k. The contribution of d_k in the probabilty P_u of undetected errors is based on the cummulative error probabilities of other distances $> d_k$ to yield a correct symbol and on the probabilities of d_k and those of other distances $< d_k$ to yield an incorrect symbol (as defined in (12)). This is mathematically expressed as:

$$\begin{aligned} P_{|d_k} = {} & (\xi)_{|d_M} \times (\xi)_{|d_{M-1}} \times \cdots \times (\xi)_{|d_{k+1}} \\ & \times \delta_k (1 - \varepsilon)_{|d_k} \times (1 - \varepsilon)_{|d_{k-1}} \times \cdots \times (1 - \varepsilon)_{|d_m}, \end{aligned} \tag{14}$$

where $(.)_{|d_k}$ is the computation of $(.)$ due to distance d_k.

By computing all the $P_{|d_k}$ values for every possible d_k defined in (5), the expression in (14) reduces to a generalised expression for the probability of undetected errors P_u in a PC system as:

$$P_u = \sum_{k=m}^{M} \delta_k \xi^k (1 - \varepsilon)^{M-k}. \tag{15}$$

The expression in (15) can work for every type of channel, provided that ε, associated with such a channel, can be computed. The computation of ε is what gives the characteristics of the communication channel. If ε for a PLC channel can be obtained, it can be substituted into (15), thereby providing a means of analysing the performance of any PC codebook $\mathcal{C}(n, M, \eta)$ over a PLC channel, provided its HDD is known. This shall therefore lead us to the computation of ε for a PLC channel impaired with impulsive noise, which is one of the most notorious noise types in PLC.

Impulsive noise has a broadband power spectral density (PSD), which sometimes affects frequency components of the transmitted data for a particular length of time. According to the approximated form of Middleton's class A noise model, it has a strength Γ, which is the relationship between its variance σ_I^2 and that of additive white Gausian noise (AWGN) σ_g^2, given by $\Gamma = \sigma_g^2/\sigma_I^2$ [6, 27]. The smaller Γ is, the more severe the impulsive noise effect becomes. If A is the probability of impulsive noise affecting a symbol, the general form of error probability for an MPSK system is modified to account for the combination of AWGN and impulsive noise effects as follows:

$$\begin{aligned} \varepsilon_{\mathrm{MPSK}} = {} & \frac{(1 - A)}{\beta} Q\left(\sqrt{\frac{\beta E_b}{\sigma_g^2}} \sin(\pi / M_{\mathrm{DP}}) \right) \\ & + \frac{A}{\beta} Q\left(\sqrt{\frac{\beta E_b}{\sigma_g^2 + \sigma_g^2/(A\Gamma)}} \sin(\pi / M_{\mathrm{DP}}) \right), \end{aligned} \tag{16}$$

where $\beta = \gamma(\log_2(M))$ and $Q(.)$ is a Q function.

For a PLC system impaired with impulsive and background noise, ε in (15) is substituted with $\varepsilon_{\mathrm{MPSK}}$. The value of γ, given by $\gamma = n/M$ is for coding rate compensation.

5 HDDs OF SOME KNOWN PCs AND THEIR PERFORMANCE RANKINGS

In order to validate the authenticity of the proposed ranking method, we adopt a number of codebooks from the available literature on PCs. As a form of evaluation, the expression in (16) was used to generate transmission errors for the expression in (15), which in turn, was used to simulate performance ranking curves for each codebook evaluated. An impulsive noise probability $A = 0.01$ was used, with varying strength Γ from 0 to 0.3.

According to [18], (3) and two other codebooks were proven to be distance optimal. We therefore consider

Table 1: Comparison of $M = 4$ PC mappings

Code	δ_2	δ_3	δ_4	Source
$\mathcal{H}_A$	64	64	112	(3), [18, (9)]
$\mathcal{H}_B$	64	64	112	[18, (8)]
$\mathcal{H}_C$	64	64	112	[18, (10)]
$\mathcal{H}_D$	72	84	84	[18, (11)]

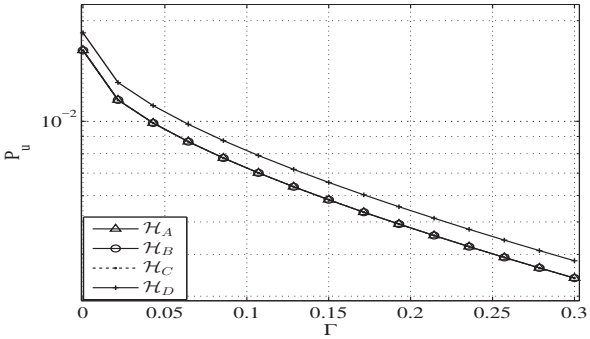


Figure 2: Performance ranking curves for Schemes $\mathcal{H}_A$ to $\mathcal{H}_D$.

another non-optimal PC of $M = 4$ and $|\mathcal{C}| = 16$ (i.e., (8) from [18]), in comparison with the optimal ones. Table 1 gives their HDDs, while their performance ranking curves, simulated from (15) and (16), are as shown in Figure 2.

According to Figure 2, code $\mathcal{H}_D$, has the worst performance. Of course, $\mathcal{H}_A$, $\mathcal{H}_B$ and $\mathcal{H}_C$ are expected to have overlapping performances, as their ranking curves clearly show, although their codewords are different. This agrees with the findings in [18]. This shall also be validated in our simulation section.

We proceed to consider PCs of $M = 5$. Here we adopt the codebook in (12) of [18] and two other similar codebooks $M(5,5,0)$ and $M(5,5,0)^*$ from [17, Appendix B.1] and denote these three codebooks as $\mathcal{J}_A$, $\mathcal{J}_B$ and $\mathcal{J}_C$. These codebooks all have $M = 5$ and $|\mathcal{C}| = 32$. According to the distance optimality approach in [17] and [18], none of these codebooks are optimal, but $\mathcal{J}_C$ is near optimal. However, what makes $\mathcal{J}_B$ and $\mathcal{J}_C$ different from $\mathcal{J}_A$ is the fact that they have some repeating permutation symbols in some of their codewords. The HDDs of these codebooks are as shown in Table 2, with their ranking curves in Figure 3.

The curves in Figure 3 show that $\mathcal{J}_A$ should have the worst

Table 2: Comparison of $M = 5$ PC mappings

Code	δ_2	δ_3	δ_4	δ_5	Source
$\mathcal{J}_A$	176	224	368	224	[18, (12)]
$\mathcal{J}_B$	160	192	384	256	[17, $M(5,5,0)$]
$\mathcal{J}_C$	160	176	352	304	[17, $M(5,5,0)^*$]

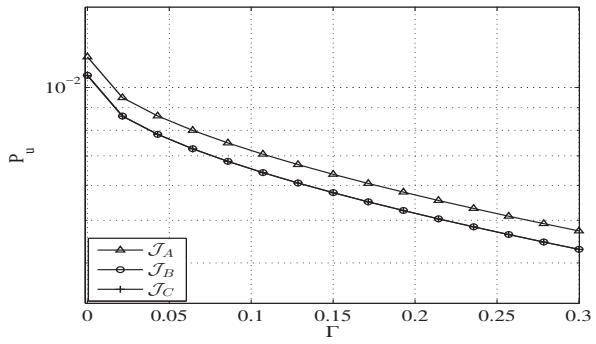


Figure 3: Performance ranking curves for Schemes $\mathcal{J}_A$ to $\mathcal{J}_C$.

Table 3: Comparison of $M = 6$ PC mappings

Code	δ_2	δ_3	δ_4	δ_5	δ_6
$\mathcal{K}_A$	320	256	896	896	1664
$\mathcal{K}_B$	320	320	736	1024	1632
$\mathcal{K}_C$	320	256	960	768	1728

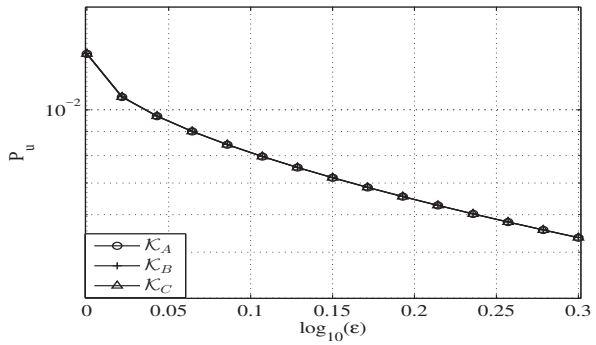


Figure 4: Performance ranking curves for Schemes $\mathcal{K}_A$ to $\mathcal{K}_C$.

performance compared to the others, which agrees with the claims in [17] and [18]. Although the findings in [17] show that $\mathcal{J}_C$ is closer to optimal than $\mathcal{J}_B$, this analysis however shows that $\mathcal{J}_B$ and $\mathcal{J}_C$ should have overlapping behaviours, which shall later be validated in the simulation section.

Next, we consider the three near-optimal codebooks, with $M = 6$, $d_m = 2$ and $|\mathcal{C}| = 64$, presented in [17]. As observed in [17], these codebooks have the same level of optimality. Their HDDs are presented in Table 3, as schemes $\mathcal{K}_A$, $\mathcal{K}_B$ and $\mathcal{K}_C$, while Figure 4 presents their ranking curves.

Based on the curves in Figure 4, all the three codebooks $\mathcal{K}_A$, $\mathcal{K}_B$ and $\mathcal{K}_C$ should have relatively overlapping performances. This is because their P_u values in Figure 4 are the same. This finding actually corroborates the notion of the optimum distance approach presented in [17].

Another set of codebooks to be considered are the four optimal codebooks, with $M = 8$, $d_m = 2$ and $|\mathcal{C}| = 256$

Table 4: Comparison of $M = 8$ PC mappings

Code	δ_2	δ_3	δ_4	δ_5	δ_6	δ_7	δ_8
$\mathcal{L}_A$	1536	1024	3584	4096	7680	7168	40192
$\mathcal{L}_B$	1024	0	5632	0	17408	0	41216
$\mathcal{L}_C$	1024	512	3072	3072	10240	12800	34560
$\mathcal{L}_D$	1536	1024	4096	4096	6656	7168	40704

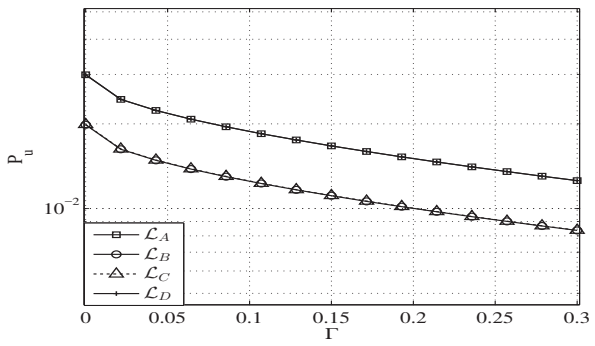


Figure 5: Performance ranking curves for Schemes $\mathcal{L}_A$ to $\mathcal{L}_D$.

Table 5: HDDs for other mappings from [17]

Code	δ_2	δ_3	δ_4	δ_5	δ_6	δ_7
$\mathcal{M}_A$	768	640	1920	1536	4352	7040
$\mathcal{M}_B$	768	640	2432	3072	5888	3456
$\mathcal{M}_C$	896	1280	3456	4864	4224	1536

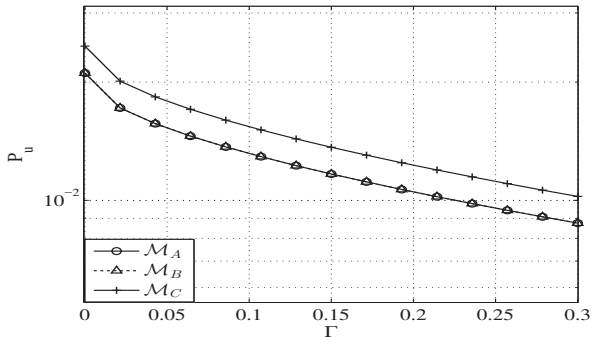


Figure 6: Performance ranking curves for Schemes $\mathcal{M}_A$ to $\mathcal{M}_C$.

in [17]. Their HDDs and ranking curves are presented in Table 4 and Figure 5, respectively.

According to the ranking curves of these codebooks, we see that $\mathcal{L}_A$ and $\mathcal{L}_D$ have overlapping curves, hence their real performances should follow a similar trend. Also, for $\mathcal{L}_B$ and $\mathcal{L}_C$, the same applies because of their overlapping performance ranking curves. Despite the fact that the four codebooks are declared optimal, our ranking method is able to determine the best from these sets of codebooks of the same class.

Further analyses carried out on some other mappings adopted from [17], are presented in Table 5 and Figure 6, based on the proposed ranking method.

Scheme $\mathcal{M}_A$ is the $M(7,7,0)$ DPM with $M = 7$, $d_m = 2$ and $|\mathcal{C}| = 128$ from [17, Appendix B.1]. Schemes $\mathcal{M}_B$ and $\mathcal{M}_C$ from [17, Appendix C.1] are also of the same class with this $M(7,7,0)$ mapping. According to [17], $\mathcal{M}_A$ is more optimal than the rest of these mappings, while $\mathcal{M}_C$ is the least optimal. However, according to their ranking curves presented in Figure 6, $\mathcal{M}_A$ and $\mathcal{M}_B$ should have overlapping performances in reality, because their curves overlap, while $\mathcal{M}_C$ should perform worse than the rest.

6 SIMULATION RESULTS AND DISCUSSION

With a view to validating the proposed ranking method, all the schemes whose HDDs and ranking curves have been presented in Tables 1 to 5 and Figures 2 to 6, were simulated under combined AWGN and impulsive noise associated with PLC channels. The input data is composed of 9600 random bits. In order to model the effect of impulsive noise on the transmitted information, we assumed a Gilbert-Elliot model, where probabilities of moving from the bad state to good state and from the good state to bad state are defined. The probability that a transmitted symbol is hit by impulsive noise, in a bad state was assumed to be $IN = 1/32$, while a good state was assumed to be free of impulsive noise. Details about this model is available in [6]. The E_b/N_o considered in the channel ranges from 0 to 25 dB.

The results shown in Figures 7 to 10 are for all the codebooks considered in our evaluations. As displayed in these figures, all the simulation results agree with the predicted performance rankings presented in Section 5. As predicted in Figure 2, Scheme $\mathcal{H}_D$ has the worst curve, which is the reason why it has the worst performance according to Figure 7. Also, the performance curves of Schemes $\mathcal{H}_A$, $\mathcal{H}_B$ and $\mathcal{H}_C$ are seen to overlap, which is in line with the prediction of the proposed ranking method. The fact that these four schemes have the same d_m does not mean they have the same performance. With the use of the proposed ranking method, we are able to know that Scheme $\mathcal{H}_D$ is not to be used in a transceiver design when codes such as $\mathcal{H}_A$, $\mathcal{H}_B$ and $\mathcal{H}_C$ are available.

The behaviours of Schemes $\mathcal{J}_A$ to $\mathcal{J}_C$ are also in the order of their ranking curves, with $\mathcal{J}_C$ and $\mathcal{J}_B$ being the best, while $\mathcal{J}_A$ is the worst, as the results in Figure 8 show. More so, as shown in Figure 9 the similarities in the performances of Schemes $\mathcal{K}_A$ to $\mathcal{K}_C$ also obey the predicted rankings presented in Figure 4.

In line with the predicted rankings in Figure 5, Schemes $\mathcal{L}_A$ and $\mathcal{L}_D$ are seen to have closely overlapping curves, especially at $E_b/N_o > 15$ dB, as shown in Figure 10. Schemes $\mathcal{L}_B$ and $\mathcal{L}_C$ also have similar patterns of behaviour, as predicted by the ranking method.

The results of the simulations done on Schemes $\mathcal{M}_A$, $\mathcal{M}_B$ and $\mathcal{M}_C$ are presented in Figure 11. According to this

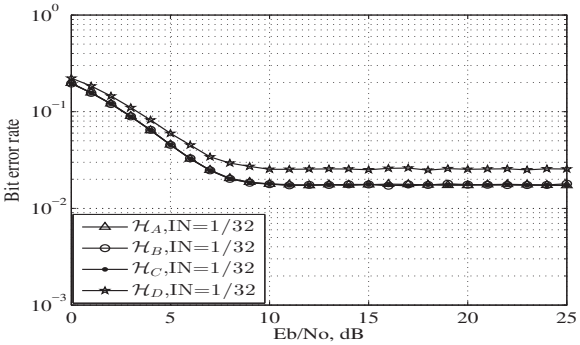


Figure 7: Bit error rate curves for Schemes $\mathcal{H}_\mathrm{A}$ to $\mathcal{H}_\mathrm{D}$, under AWGN+impulsive noise channel.

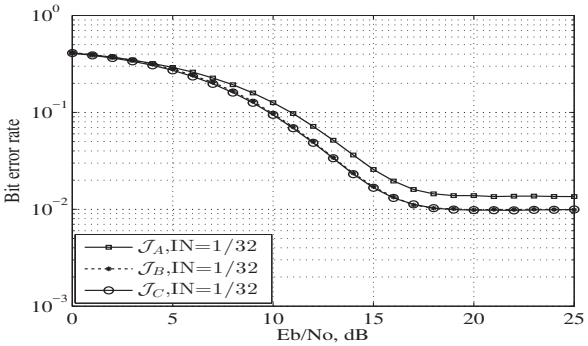


Figure 8: Bit error rate curves for Schemes $\mathcal{J}_\mathrm{A}$ to $\mathcal{J}_\mathrm{C}$, under AWGN+impulsive noise channel.

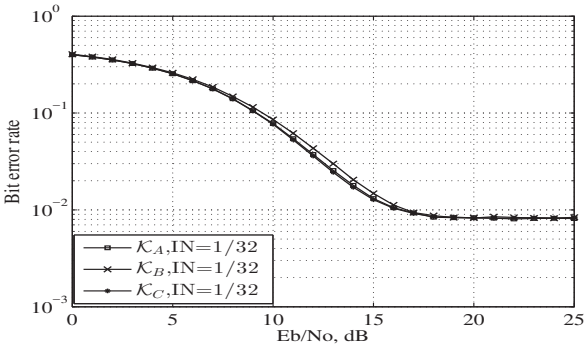


Figure 9: Bit error rate curves for Schemes $\mathcal{K}_\mathrm{A}$ to $\mathcal{K}_\mathrm{C}$, under AWGN+impulsive noise channel.

figure, $\mathcal{M}_\mathrm{A}$ is seen to overlap with $\mathcal{M}_\mathrm{B}$, but at high E_b/N_o values, while $\mathcal{M}_\mathrm{C}$ is seen to be the worst performing scheme. This is in agreement with the predicted rankings presented in Figure 6, based on the proposed ranking method.

In the above simulation results, it is worth noting that the probability *IN* used in the impulsive noise model is considered very high. That is why the performances of all the codebooks presented are relatively poor. With the aid of interleaving and concatenated outer codes, such as Reed-Solomon codes, the performances will definitely improve. Although the codebooks evaluated have a $d_m =$

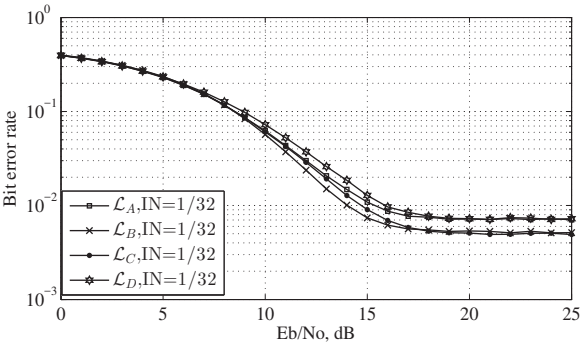


Figure 10: Bit error rate curves for Schemes $\mathcal{L}_\mathrm{A}$ to $\mathcal{L}_\mathrm{D}$, under AWGN+impulsive noise channel.

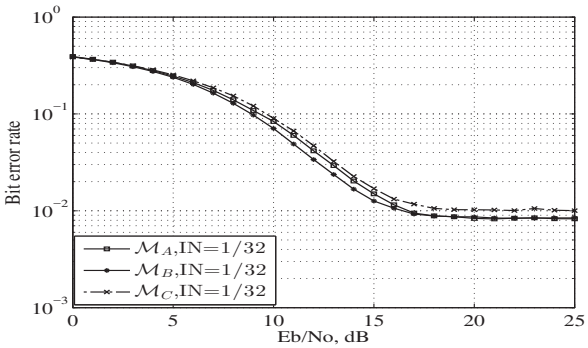


Figure 11: Bit error rate curves for Schemes $\mathcal{M}_\mathrm{A}$ to $\mathcal{M}_\mathrm{C}$, under AWGN+impulsive noise channel.

2, it does not mean that the proposed ranking method is limited to such cases. The method can be applied to any codebook category. Also, the significance of the different behaviours of all the schemes considered, are best observed at high E_b/N_o values.

7 CONCLUSION

Permutation coding has emerged as a promising channel coding scheme in PLC related applications. With a view to contributing to this field, we have presented a fast and simple way of ranking the relative performance of PC codebooks with similar properties. This method computes the Hamming distance distribution of the PC codebook and uses the information therein to compute the probability P_u of undetected error, which can, in turn, be used to compare the codebook to other codebooks with similar properties. A codebook with lower P_u values has better performance than any codebook with higher P_u values.

The method was validated using various known PC codebooks adopted from literature. The results of the simulations carried out agree with our claims, when the proposed method was used as a performance ranking tool. This tool is useful, when an efficient codebook is to be selected out of a number of similar codebooks. More so, it can be incorporated when exhaustive search for codebooks is done. It should however be noted that the computation of P_u considers only AWGN and impulsive noise effects.

An extended work in this area of study can be centered on including the effects of other types of PLC noise, such as narrowband noise in the computation of probability P_u. This, however remains a challenge as there is no link found between its PSD and that of AWGN.

ACKNOWLEDGEMENT

This work is based on research supported in part by the National Research Foundation of South Africa (UID 77596).

REFERENCES

[1] A.J.H. Vinck and J. Häring. "Coding and modulation for power-line communications," in *Proceedings of the 2000 IEEE International Symposium on Power Line Communications and its Applications*, Limerick, Apr. 2000, pp. 265–71.

[2] H.C. Ferreira, H.M. Grové, O. Hooijen and A.J.H. Vinck, "Power line communication," *Wiley Encyclopedia of Electrical and Electronics Engineering*, 2001.

[3] eRDF, *PLC G3 Physical Layer Specification*, 2013.

[4] CENELEC, *50065 part 1: Signalling on low voltage electrical installations in the frequency range 3 kHz to 148.5 kHz, general requirments, frequency bands and electromagnetic disturbances*, 1992.

[5] PRIME, *PRIME Technology, whitepaper: PHY, MAC and Convergence layers*, 21st Ed., 2008.

[6] V.N. Papilaya, T. Shongwe, A.J.H. Vinck and H.C. Ferreira, "Selected subcarriers QPSK-OFDM transmission schemes to combat frequency disturbances," in *Proceedings of the 2012 IEEE International Symposium on Power Line Communications and its Applications*, Beijing, Mar. 2012, pp. 200–5.

[7] H.C. Ferreira, A.J.H. Vinck, T.G. Swart and I. de Beer, "Permutation trellis codes," *IEEE Transactions on Commununications*, Vol. 53, pp. 1782–9, Nov. 2005.

[8] T.G. Swart and H.C. Ferreira. "Decoding distance-preserving permutation codes for power-line communications," in *Proceedings of IEEE AFRICON*, Windhoek, Sept. 2007, pp. 1–7.

[9] K. Ogunyanda, A.D. Familua, T.G. Swart, H.C. Ferreira and L. Cheng, "Evaluation and implementation of cyclic permutation coding for power line communications," in *Proceedings of the 2014 IEEE International Conference on Adaptive Science & Technology (ICAST)*, Ota, Oct. 2014, pp. 1–7.

[10] P.J. Dukes, "Coding with injections," *Designs, Codes and Cryptography*, Vol. 65, pp. 213–22, Dec. 2012.

[11] F.H. Hunt, S. Perkins and D.H. Smith, "Decoding mixed errors and erasures in permutation codes," *Designs, Codes and Cryptography*, Vol. 74, pp. 481–93, Feb. 2015.

[12] S. Huczynska and G.L. Mullen, "Frequency permutation arrays," *Journal of Combinatorial Designs*, Vol. 14, pp. 463–78, Jan. 2006.

[13] R.F. Bailey, "Error-correcting codes from permutation groups," *Discrete Mathematics*, Vol. 309, pp. 4253–65, 2009.

[14] K. Ogunyanda, A.D. Familua, T.G. Swart, H.C. Ferreira and L. Cheng, "Permutation coding with differential quinary phase shift keying for power line communication," in *Proceedings of the 2014 IEEE PES Innovative Smart Grid Technologies European Conference*, Istanbul, Oct. 2014, pp. 1–6.

[15] H.C. Ferreira and A.J.H. Vinck, "Interference cancellation with permutation trellis codes," in *Proceedings of the 2000 IEEE Vehicular Technology Conference*, Boston, MA, Sep. 2000, pp. 2401-7.

[16] Y.M. Chee, H.M. Kia, P. Purkayastha and C. Wang, "Importance of symbol equity in coded modulation for power line communications," in *Proceedings of the 2012 IEEE International Symposium on Information Theory*, Cambridge, Jul. 2012, pp. 661–5.

[17] T.G. Swart, "Distance-preserving mappings and trellis codes with permutation sequences," Ph.D. dissertation, University of Johannesburg, 2006.

[18] T.G. Swart, I. de Beer and H.C. Ferreira, "On the distance optimality of permutation mappings," in *Proceedings of the 2005 IEEE International Symposium on Information Theory*, Adelaide, Sept. 2005, pp. 1068–72.

[19] A.J. Viterbi, "Convolutional codes and their performance in communication systems," *IEEE Transactions on Communications Technology*, Vol. 19, pp. 751–72, Oct. 1971.

[20] G.A. Alexandre, M. Guido and B. Sergio, "A new approach to the construction of high-rate convolutional codes," *IEEE Communications Letters*, Vol. 5, pp. 453–5, Nov. 2001.

[21] B.F. Ucha-Filho, R.D. Souza, C. Pimentel and M. Jar, "Further results on convolutional codes based on a minimal trellis complexity measure," in *Proceedings of the 2006 IEEE International Telecommunication Symposium*, Fortalez, Sept. 2006, pp. 123–8.

[22] Y. Bian, A. Popplewell and J.J. O'Reilly, "New very high rate punctured convolutional codes," *Electronics Letters*, Vol. 30, pp. 1119–20, Jul. 1994.

[23] T. Wadayama and M. Hagiwara, "LP-decodable permutation codes based on linearly constrained permutation matrices," *IEEE Transactions on Information Theory*, Vol. 58, pp. 5454–70, Aug. 2012.

[24] V.B. Balakirsky and A.J.H. Vinck, "Potential limits on power-line communication over impulsive noise channels," in *Proceedings of the 2003 IEEE International Symposium on Power Line Communications and its Applications*, Kyoto, Mar. 2003, pp. 32–7.

[25] J.G. Proakis, *Digital Communications*, McGraw-Hill, 4th edition, Chapter 7, pp. 364–412, 2001.

[26] T.G. Swart and H.C. Ferreira, "A generalised upper bound and a multilevel construction for distance-preserving mappings," *IEEE Transactions on Information Theory*, Vol. 52, pp. 3685–95, Aug. 2006.

[27] T. Shongwe, A.J.H. Vinck and H.C. Ferreira, "On impulse noise and its models," *Proceedings of the 2014 IEEE International Symposium on Power Line Communications and its Applications*, Glasgow, Mar. 2014, pp. 12–7.

APPENDIX

Codes for Schemes $\mathcal{H}_A$ to $\mathcal{H}_D$:

$$\mathcal{H}_{\mathrm{A}} = \left\{ \begin{array}{c} 1230, 1203, 1320, 1302, 2130, 2103, 3120, 3102 \\ 0231, 0213, 0321, 0312, 2031, 2013, 3021, 3012 \end{array} \right\}$$

$$\mathcal{H}_{\mathrm{B}} = \left\{ \begin{array}{c} 1230, 1203, 1320, 1302, 0231, 0213, 0321, 0312 \\ 2130, 2103, 3120, 3102, 2031, 2013, 3021, 3012 \end{array} \right\}$$

$$\mathcal{H}_{\mathrm{C}} = \left\{ \begin{array}{c} 1230, 1203, 2130, 2103, 1320, 1302, 3120, 3102 \\ 0231, 0213, 2031, 2013, 0321, 0312, 3021, 3012 \end{array} \right\}$$

$$\mathcal{H}_{\mathrm{D}} = \left\{ \begin{array}{c} 1230, 1203, 1320, 1302, 1023, 1032, 2130, 2103 \\ 3210, 3201, 2310, 2301, 3021, 3012, 3120, 3102 \end{array} \right\}$$

Codes for Schemes $\mathcal{J}_A$ to $\mathcal{J}_C$:

$$\mathcal{J}_{\mathrm{A}} = \left\{ \begin{array}{c} 01234, 01243, 01324, 01342, 01423, 01432 \\ 02134, 02143, 03214, 03241, 02314, 02341 \\ 03421, 03412, 03124, 03142, 41230, 41203 \\ 41320, 41302, 41023, 41032, 42130, 42103 \\ 43210, 43201, 42310, 42301, 43021, 43012 \\ 43120, 43102 \end{array} \right\}$$

$$\mathcal{J}_{\mathrm{B}} = \left\{ \begin{array}{c} 12340, 21340, 12430, 21430, 32140, 31240 \\ 42130, 41230, 14320, 24310, 13420, 23410 \\ 34120, 34210, 43120, 43210, 02341, 01342 \\ 02431, 01432, 02143, 01243, 02134, 01234 \\ 04321, 04312, 03421, 03412, 04123, 04213 \\ 03124, 03214 \end{array} \right\}$$

$$\mathcal{J}_{\mathrm{C}} = \left\{ \begin{array}{c} 04321, 03421, 04312, 03412, 40321, 30421 \\ 40312, 30412, 02341, 02431, 01342, 01432 \\ 42301, 32401, 41302, 31402, 04123, 03124 \\ 04213, 03214, 40123, 30124, 40213, 30214 \\ 02143, 02134, 01243, 01234, 42103, 32104 \\ 41203, 31204 \end{array} \right\}$$

Codes for Schemes $\mathcal{K}_A$ to $\mathcal{K}_C$:

$$\mathcal{K}_{\mathrm{A}} = \left\{ \begin{array}{c} 123450, 213450, 124350, 214350, 123405 \\ 213405, 124305, 214305, 321450, 312450 \\ 421350, 412350, 321405, 312405, 421305 \\ 412305, 143250, 243150, 134250, 234150 \\ 143205, 243105, 134205, 234105, 341250 \\ 342150, 431250, 432150, 341205, 342105 \\ 431205, 432105, 503412, 503421, 504312 \\ 504321, 053412, 053421, 054312, 054321 \\ 501432, 502431, 501342, 502341, 051432 \\ 052431, 051342, 052341, 503214, 503124 \\ 504213, 504123, 053214, 053124, 054213 \\ 054123, 501234, 502134, 501243, 502143 \\ 051234, 052134, 051243, 052143 \end{array} \right\}$$

$$\mathcal{K}_{\mathrm{B}} = \left\{ \begin{array}{c} 123450, 213450, 124305, 214305, 321450 \\ 312450, 421305, 412305, 143250, 243150 \\ 134205, 234105, 341250, 342150, 431205 \\ 432105, 523410, 513420, 024315, 014325 \\ 521430, 512430, 021345, 012345, 543210 \\ 543120, 034215, 034125, 541230, 542130 \\ 031245, 032145, 103452, 203451, 154302 \\ 254301, 301452, 302451, 451302, 452301 \\ 103254, 203154, 154203, 254103, 301254 \\ 302154, 451203, 452103, 503412, 503421 \\ 054312, 054321, 501432, 502431, 051342 \\ 052341, 503214, 503124, 054213, 054123 \\ 501234, 502134, 051243, 052143 \end{array} \right\}$$

$$\mathcal{K}_{\mathrm{C}} = \left\{ \begin{array}{c} 123450, 213450, 124350, 214350, 123405 \\ 213405, 124305, 214305, 341250, 342150 \\ 431250, 432150, 341205, 342105, 431205 \\ 432105, 523410, 513420, 524310, 514320 \\ 023415, 013425, 024315, 014325, 541230 \\ 542130, 531240, 532140, 041235, 042135 \\ 031245, 032145, 103452, 203451, 104352 \\ 204351, 153402, 253401, 154302, 254301 \\ 301254, 302154, 401253, 402153, 351204 \\ 352104, 451203, 452103, 503412, 503421 \\ 504312, 504321, 053412, 053421, 054312 \\ 054321, 501234, 502134, 501243, 502143 \\ 051234, 052134, 051243, 052143 \end{array} \right\}$$

Codes for Schemes $\mathcal{L}_A$ to $\mathcal{L}_D$:

$$\mathcal{L}_{\mathrm{A}} = \left\{ \begin{array}{c} 12345670, 12345607, 12346570, 12346507, 12435670, 12435607, 12436570, 12436507, 21345670 \\ 21345607, 21346570, 21346507, 21435670, 21435607, 21436570, 21436507, 12345076, 12345706 \\ 12346075, 12346705, 12435076, 12435706, 12436075, 12436705, 21345076, 21345706, 21346075 \\ 21346705, 21435076, 21435706, 21436075, 21436705, 14325670, 14325607, 14326570, 14326507 \\ 13425670, 13425607, 13426570, 13426507, 24315670, 24315607, 24316570, 24316507, 23415670 \\ 23415607, 23416570, 23416507, 14325076, 14325706, 14326075, 14326705, 13425076, 13425706 \\ 13426075, 13426705, 24315076, 24315706, 24316075, 24316705, 23415076, 23415706, 23416075 \\ 23416705, 32147650, 32140657, 32147560, 32140567, 42137650, 42130657, 42137560, 42130567 \\ 31247650, 31240657, 31247560, 31240567, 41237650, 41230657, 41237560, 41230567, 32147056 \\ 32140756, 32147065, 32140765, 42137056, 42130756, 42137065, 42130765, 31247056, 31240756 \\ 31247065, 31240765, 41237056, 41230756, 41237065, 41230765, 34127650, 34120657, 34127560 \\ 34120567, 43127650, 43120657, 43127560, 43120567, 34217650, 34210657, 34217560, 34210567 \\ 43217650, 43210657, 43217560, 43210567, 34127056, 34120756, 34127065, 34120765, 43127056 \\ 43120756, 43127065, 43120765, 34217056, 34210756, 34217065, 34210765, 43217056, 43210756 \\ 43217065, 43210765, 56701234, 56071234, 65701234, 65071234, 56701243, 56071243, 65701243 \\ 65071243, 56702134, 56072134, 65702134, 65072134, 56702143, 56072143, 65702143, 65072143 \\ 50761234, 57061234, 60751234, 67051234, 50761243, 57061243, 60751243, 67051243, 50762134 \\ 57062134, 60752134, 67052134, 50762143, 57062143, 60752143, 67052143, 56701432, 56071432 \\ 65701432, 65071432, 56701342, 56071342, 65701342, 65071342, 56702431, 56072431, 65702431 \\ 65072431, 56702341, 56072341, 65702341, 65072341, 50761432, 57061432, 60751432, 67051432 \\ 50761342, 57061342, 60751342, 67051342, 50762431, 57062431, 60752431, 67052431, 50762341 \\ 57062341, 60752341, 67052341, 76503214, 06573214, 75603214, 05673214, 76504213, 06574213 \\ 75604213, 05674213, 76503124, 06573124, 75603124, 05673124, 76504123, 06574123, 75604123 \\ 05674123, 70563214, 07563214, 70653214, 07653214, 70564213, 07564213, 70654213, 07654213 \\ 70563124, 07563124, 70653124, 07653124, 70564123, 07564123, 70654123, 07654123, 76503412 \\ 06573412, 75603412, 05673412, 76504312, 06574312, 75604312, 05674312, 76503421, 06573421 \\ 75603421, 05673421, 76504321, 06574321, 75604321, 05674321, 70563412, 07563412, 70653412 \\ 07653412, 70564312, 07564312, 70654312, 07654312, 70563421, 07563421, 70653421, 07653421 \\ 70564321, 07564321, 70654321, 07654321 \end{array} \right\}$$

$$\mathcal{L}_{\mathrm{B}} = \left\{ \begin{array}{c} 12345670, 12345607, 12346570, 12346507, 12435670, 12435607, 12436570, 12436507, 21345670 \\ 21345607, 21346570, 21346507, 21435670, 21435607, 21436570, 21436507, 12347056, 12340756 \\ 12347065, 12340765, 12437056, 12430756, 12437065, 12430765, 21347056, 21340756, 21347065 \\ 21340765, 21437056, 21430756, 21437065, 21430765, 34125670, 34125607, 34126570, 34126507 \\ 43125670, 43125607, 43126570, 43126507, 34215670, 34215607, 34216570, 34216507, 43215670 \\ 43215607, 43216570, 43216507, 34127056, 34120756, 34127065, 34120765, 43127056, 43120756 \\ 43127065, 43120765, 34217056, 34210756, 34217065, 34210765, 43217056, 43210756, 43217065 \\ 43210765, 12705634, 12075634, 12706534, 12076534, 12705643, 12075643, 12706543, 12076543 \\ 21705634, 21075634, 21706534, 21076534, 21705643, 21075643, 21706543, 21076543, 12567034 \\ 12560734, 12657034, 12650734, 12567043, 12560743, 12657043, 12650743, 21567034, 21560734 \\ 21657034, 21650734, 21567043, 21560743, 21657043, 21650743, 34705612, 34075612, 34706512 \\ 34076512, 43705612, 43075612, 43706512, 43076512, 34705621, 34075621, 34706521, 34076521 \\ 43705621, 43075621, 43706521, 43076521, 34567012, 34560712, 34657012, 34650712, 43567012 \\ 43560712, 43657012, 43650712, 34567021, 34560721, 34657021, 34650721, 43567021, 43560721 \\ 43657021, 43650721, 56341270, 56341207, 65341270, 65341207, 56431270, 56431207, 65431270 \\ 65431207, 56342170, 56342107, 65342170, 65342107, 56432170, 56432107, 65432170, 65432107 \\ 70341256, 07341256, 70341265, 07341265, 70431256, 07431256, 70431265, 07431265, 70342156 \\ 07342156, 70342165, 07342165, 70432156, 07432156, 70432165, 07432165, 56123470, 56123407 \\ 65123470, 65123407, 56124370, 56124307, 65124370, 65124307, 56213470, 56213407, 65213470 \\ 65213407, 56214370, 56214307, 65214370, 65214307, 70123456, 07123456, 70123465, 07123465 \\ 70124356, 07124356, 70124365, 07124365, 70213456, 07213456, 70213465, 07213465, 70214356 \\ 07214356, 70214365, 07214365, 56701234, 56071234, 65701234, 65071234, 56701243, 56071243 \\ 65701243, 65071243, 56702134, 56072134, 65702134, 65072134, 56702143, 56072143, 65702143 \\ 65072143, 70561234, 07561234, 70651234, 07651234, 70561243, 07561243, 70651243, 07651243 \\ 70562134, 07562134, 70652134, 07652134, 70562143, 07562143, 70652143, 07652143, 56703412 \\ 56073412, 65703412, 65073412, 56704312, 56074312, 65704312, 65074312, 56703421, 56073421 \\ 65703421, 65073421, 56704321, 56074321, 65704321, 65074321, 70563412, 07563412, 70653412 \\ 07653412, 70564312, 07564312, 70654312, 07654312, 70563421, 07563421, 70653421, 07653421 \\ 70564321, 07564321, 70654321, 07654321 \end{array} \right\}$$

$$\mathcal{L}_{\mathrm{C}} = \left\{ \begin{array}{c} 12345670, 12346507, 21435670, 21436507, 12345076, 12346705, 21435076, 21436705, 14325670 \\ 14326507, 23415670, 23416507, 14325076, 14326705, 23415076, 23416705, 32147650, 32140567 \\ 41237650, 41230567, 32147056, 32140765, 41237056, 41230765, 34127650, 34120567, 43217650 \\ 43210567, 34127056, 34120765, 43217056, 43210765, 12305674, 12376504, 21405673, 21476503 \\ 12365074, 12356704, 21465073, 21456703, 14305672, 14376502, 23405671, 23476501, 14365072 \\ 14356702, 23465071, 23456701, 32107654, 32170564, 41207653, 41270563, 32167054, 32150764 \\ 41267053, 41250763, 34107652, 34170562, 43207651, 43270561, 34167052, 34150762, 43267051 \\ 43250761, 12745630, 12046537, 21735640, 21036547, 12745036, 12046735, 21735046, 21036745 \\ 14725630, 14026537, 23715640, 23016547, 14725036, 14026735, 23715046, 23016745, 32547610 \\ 32640517, 41537620, 41630527, 32547016, 32640715, 41537026, 41630725, 34527610, 34620517 \\ 43517620, 43610527, 34527016, 34620715, 43517026, 43610725, 12705634, 12076534, 21705643 \\ 21076543, 12765034, 12056734, 21765043, 21056743, 14705632, 14076532, 23705641, 23076541 \\ 14765032, 14056732, 23765041, 23056741, 32507614, 32670514, 41507623, 41670523, 32567014 \\ 32650714, 41567023, 41650723, 34507612, 34670512, 43507621, 43670521, 34567012, 34650712 \\ 43567021, 43650721, 56341270, 65341207, 56432170, 65432107, 50341276, 67341205, 50432176 \\ 67432105, 56321470, 65321407, 56412370, 65412307, 50321476, 67321405, 50412376, 67412305 \\ 76143250, 05143267, 76234150, 05234167, 70143256, 07143265, 70234156, 07234165, 76123450 \\ 05123467, 76214350, 05214367, 70123456, 07123465, 70214356, 07214365, 56301274, 65371204 \\ 56402173, 65472103, 50361274, 67351204, 50462173, 67452103, 56301472, 65371402, 56402371 \\ 65472301, 50361472, 67351402, 50462371, 67452301, 76103254, 05173264, 76204153, 05274163 \\ 70163254, 07153264, 70264153, 07254163, 76103452, 05173462, 76204351, 05274361, 70163452 \\ 07153462, 70264351, 07254361, 56741230, 65041237, 56732140, 65032147, 50741236, 67041235 \\ 50732146, 67032145, 56721430, 65021437, 56712340, 65012347, 50721436, 67021435, 50712346 \\ 67012345, 76543210, 05643217, 76534120, 05634127, 70543216, 07643215, 70534126, 07634125 \\ 76523410, 05623417, 76514320, 05614327, 70523416, 07623415, 70514326, 07614325, 56701234 \\ 65071234, 56702143, 65072143, 50761234, 67051234, 50762143, 67052143, 56701432, 65071432 \\ 56702341, 65072341, 50761432, 67051432, 50762341, 67052341, 76503214, 05673214, 76504123 \\ 05674123, 70563214, 07653214, 70564123, 07654123, 76503412, 05673412, 76504321, 05674321 \\ 70563412, 07653412, 70564321, 07654321 \end{array} \right\}$$

$$\mathcal{L}_{\mathrm{D}} = \left\{ \begin{array}{c} 12345670, 21436507, 12345076, 21436705, 14325670, 23416507, 14325076, 23416705, 32147650 \\ 41230567, 32147056, 41230765, 34127650, 43210567, 34127056, 43210765, 12305674, 21476503 \\ 12365074, 21456703, 14305672, 23476501, 14365072, 23456701, 32107654, 41270563, 32167054 \\ 41250763, 34107652, 43270561, 34167052, 43250761, 12745630, 21036547, 12745036, 21036745 \\ 14725630, 23016547, 14725036, 23016745, 32547610, 41630527, 32547016, 41630725, 34527610 \\ 43610527, 34527016, 43610725, 12705634, 21076543, 12765034, 21056743, 14705632, 23076541 \\ 14765032, 23056741, 32507614, 41670523, 32567014, 41650723, 34507612, 43670521, 34567012 \\ 43650721, 15342670, 26431507, 15342076, 26431705, 15324670, 26413507, 15324076, 26413705 \\ 37142650, 40231567, 37142056, 40231765, 37124650, 40213567, 37124056, 40213765, 15302674 \\ 26471503, 15362074, 26451703, 15304672, 26473501, 15364072, 26453701, 37102654, 40271563 \\ 37162054, 40251763, 37104652, 40273561, 37164052, 40253761, 15742630, 26031547, 15742036 \\ 26031745, 15724630, 26013547, 15724036, 26013745, 37542610, 40631527, 37542016, 40631725 \\ 37524610, 40613527, 37524016, 40613725, 15702634, 26071543, 15762034, 26051743, 15704632 \\ 26073541, 15764032, 26053741, 37502614, 40671523, 37562014, 40651723, 37504612, 40673521 \\ 37564012, 40653721, 62345170, 51436207, 02345176, 71436205, 64325170, 53416207, 04325176 \\ 73416205, 62147350, 51230467, 02147356, 71230465, 64127350, 53210467, 04127356, 73210465 \\ 62305174, 51476203, 02365174, 71456203, 64305172, 53476201, 04365172, 73456201, 62107354 \\ 51270463, 02167354, 71250463, 64107352, 53270461, 04167352, 73250461, 62745130, 51036247 \\ 02745136, 71036245, 64725130, 53016247, 04725136, 73016245, 62547310, 51630427, 02547316 \\ 71630425, 64527310, 53610427, 04527316, 73610425, 62705134, 51076243, 02765134, 71056243 \\ 64705132, 53076241, 04765132, 73056241, 62507314, 51670423, 02567314, 71650423, 64507312 \\ 53670421, 04567312, 73650421, 65342170, 56431207, 05342176, 76431205, 65324170, 56413207 \\ 05324176, 76413205, 67142350, 50231467, 07142356, 70231465, 67124350, 50213467, 07124356 \\ 70213465, 65302174, 56471203, 05362174, 76451203, 65304172, 56473201, 05364172, 76453201 \\ 67102354, 50271463, 07162354, 70251463, 67104352, 50273461, 07164352, 70253461, 65742130 \\ 56031247, 05742136, 76031245, 65724130, 56013247, 05724136, 76013245, 67542310, 50631427 \\ 07542316, 70631425, 67524310, 50613427, 07524316, 70613425, 65702134, 56071243, 05762134 \\ 76051243, 65704132, 56073241, 05764132, 76053241, 67502314, 50671423, 07562314, 70651423 \\ 67504312, 50673421, 07564312, 70653421 \end{array} \right\}$$

Codes for Schemes $\mathcal{M}_A$ to $\mathcal{M}_D$:

$$\mathcal{M}_{\mathrm{A}} = \left\{ \begin{array}{c} 1234567, 2134567, 1243567, 2143567, 1234657, 2134657, 1243657, 2143657, 3214567, 3124567 \\ 4213567, 4123567, 3214657, 3124657, 4213657, 4123657, 1432567, 2431567, 1342567, 2341567 \\ 1432657, 2431657, 1342657, 2341657, 3412567, 3421567, 4312567, 4321567, 3412657, 3421657 \\ 4312657, 4321657, 1234765, 2134765, 1243765, 2143765, 1234756, 2134756, 1243756, 2143756 \\ 3214765, 3124765, 4213765, 4123765, 3214756, 3124756, 4213756, 4123756, 1432765, 2431765 \\ 1342765, 2341765, 1432756, 2431756, 1342756, 2341756, 3412765, 3421765, 4312765, 4321765 \\ 3412756, 3421756, 4312756, 4321756, 5674123, 5674213, 5673124, 5673214, 6574123, 6574213 \\ 6573124, 6573214, 5674321, 5674312, 5673421, 5673412, 6574321, 6574312, 6573421, 6573412 \\ 5672143, 5671243, 5672134, 5671234, 6572143, 6571243, 6572134, 6571234, 5672341, 5671342 \\ 5672431, 5671432, 6572341, 6571342, 6572431, 6571432, 7654123, 7654213, 7653124, 7653214 \\ 7564123, 7564213, 7563124, 7563214, 7654321, 7654312, 7653421, 7653412, 7564321, 7564312 \\ 7563421, 7563412, 7652143, 7651243, 7652134, 7651234, 7562143, 7561243, 7562134, 7561234 \\ 7652341, 7651342, 7652431, 7651432, 7562341, 7561342, 7562431, 7561432 \end{array} \right\}$$

$$\mathcal{M}_{\mathrm{B}} = \left\{ \begin{array}{c} 1234566, 2134566, 1243566, 2143566, 1234656, 2134656, 1243656, 2143656, 3412566, 3421566 \\ 4312566, 4321566, 3412656, 3421656, 4312656, 4321656, 5234166, 5134266, 5243166, 5143266 \\ 6234156, 6134256, 6243156, 6143256, 5412366, 5421366, 5312466, 5321466, 6412356, 6421356 \\ 6312456, 6321456, 1634526, 2634516, 1643526, 2643516, 1534626, 2534616, 1543626, 2543616 \\ 3612546, 3621546, 4612536, 4621536, 3512646, 3521646, 4512636, 4521636, 5634126, 5634216 \\ 5643126, 5643216, 6534126, 6534216, 6543126, 6543216, 5612346, 5621346, 5612436, 5621436 \\ 6512346, 6521346, 6512436, 6521436, 1264563, 2164563, 1263564, 2163564, 1264653, 2164653 \\ 1263654, 2163654, 3462561, 3461562, 4362561, 4361562, 3462651, 3461652, 4362651, 4361652 \\ 5264163, 5164263, 5263164, 5163264, 6264153, 6164253, 6263154, 6163254, 5462361, 5461362 \\ 5362461, 5361462, 6462351, 6461352, 6362451, 6361452, 1664523, 2664513, 1663524, 2663514 \\ 1564623, 2564613, 1563624, 2563614, 3662541, 3661542, 4662531, 4661532, 3562641, 3561642 \\ 4562631, 4561632, 5664123, 5664213, 5663124, 5663214, 6564123, 6564213, 6563124, 6563214 \\ 5662341, 5661342, 5662431, 5661432, 6562341, 6561342, 6562431, 6561432 \end{array} \right\}$$

$$\mathcal{M}_{\mathrm{C}} = \left\{ \begin{array}{c} 1234555, 2134555, 1243555, 2143555, 1254553, 2154553, 1253554, 2153554, 3214555.3124555 \\ 4213555, 4123555, 3254551, 3154552, 4253551, 4153552, 1432555, 2431555, 1342555, 2341555 \\ 1452553, 2451553, 1352554, 2351554, 3412555, 3421555, 4312555, 4321555, 3452551, 3451552 \\ 4352551, 4351552, 5234155, 5134255, 5243155, 5143255, 5254153, 5154253, 5253154, 5153254 \\ 5214355, 5124355, 5213455, 5123455, 5254351, 5154352, 5253451, 5153452, 5432155, 5431255 \\ 5342155, 5341255, 5452153, 5451253, 5352154, 5351254, 5412355, 5421355, 5312455, 5321455 \\ 5452351, 5451352, 5352451, 5351452, 1534525, 2534515, 1543525, 2543515, 1554523, 2554513 \\ 1553524, 2553514, 3514525, 3524515, 4513525, 4523515, 3554521, 3554512, 4553521, 4553512 \\ 1532545, 2531545, 1542535, 2541535, 1552543, 2551543, 1552534, 2551534, 3512545, 3521545 \\ 4512535, 4521535, 3552541, 3551542, 4552531, 4551532, 5534125, 5534215, 5543125, 5543215 \\ 5554123, 5554213, 5553124, 5553214, 5514325, 5524315, 5513425, 5523415, 5554321, 5554312 \\ 5553421, 5553412, 5532145, 5531245, 5542135, 5541235, 5552143, 5551243, 5552134, 5551234 \\ 5512345, 5521345, 5512435, 5521435, 5552341, 5551342, 5552431, 5551432 \end{array} \right\}$$

THE MODIFIED SOFT INPUT PARITY CHECK TRANSFORMATION ALGORITHM FOR REED SOLOMON CODES

Y. Genga , D.J.J. Versfeld*

* *School of Electrical and Information Engineering,University of the Witwatersrand, Private Bag 3, Wits 2050, Johannesburg, South Africa. E-mail: yuval.genga@students.wits.ac.za, and jaco.versfeld@wits.ac.za.*

Abstract: In this paper, we propose a modification to the recently developed Parity check Transformation Algorithm (PTA) used in the decoding of Reed Solomon codes. This extension of the PTA is referred to as the Modified Parity check Transformation Algorithm (MPTA). The MPTA is developed with the aim of reducing the number of iterations run by the algorithm during the decoding process, and also to improve on the SER performance of the algorithm. Three version of the MPTA are developed in this paper to achieve this goal.

Key words: Reed Solomon codes, Soft decision decoding, Iterative decoding.

1. INTRODUCTION

Reed-Solomon (*RS*) codes [1] are a class of linear block codes that are widely used for applications that range from telecommunications to storage devices. These codes are largely popular because they meet the Singleton bound. What this means is that a hard decision decoder (HDD) based on minimum distance decoding can correct up to $[n-k]/2$ symbols for a given (n,k) *RS* code. Hard decision decoders for *RS* codes include the Berlekamp-Massey (*B-M*) algorithm [2] [3], the Euclidean algorithm [4], and the Berlekamp-Welch algorithm [5]. HDD algorithms for *RS* codes have been shown to be efficient, however, they are significantly outperformed by soft decision decoding techniques.

Koetter and Vardy (*KV*) [6] presented a symbol level decoding algorithm that utilizes the soft reliability information from the channel to make a multiplicity matrix that is fed into the Guruswami Sudan (*GS*) [7] algorithm. The *KV* algorithm outperforms HDD algorithms significantly especially for low rate codes. However, complexity can become prohibitively large when trying to achieve large coding gains with the *KV* algorithm [8].

The Parity check Transformation Algorithm (PTA) is a symbol wise soft decision decoding algorithm that was recently proposed in [9]. The algorithm transforms the parity check matrix, H, of an *RS* code after every iteration depending on the reliability of the symbols. The reliability of the symbols are attained from soft information received at the channel output. In the same paper, the PTA algorithm was shown to outperform the widely used Koetter and Vardy (*KV*) algorithm and the Berlekamp-Massey (BM) algorithm for simulations run in the AWGN channel with the symbols being mapped onto a 16QAM modulation scheme. The performance was measured in terms of the symbol error rate (SER). The major drawback of the PTA is the high number of iterations needed to find the decoded codeword, especially for low SNR cases.

In this paper, modifications to the PTA are introduced with the aim of reducing the number of iterations required to decode. These modifications are used to develop an extension of the PTA, which is referred to as the Modified PTA (MPTA)

The rest of the paper is structured as follows. A basic description of how the PTA decoding algorithm works is given in Section 2. The analysis and modifications to the PTA is explained Section 3. A performance comparison between the PTA and the MPTA algorithms is done in Section 4. Finally, a conclusion is given in Section 5.

2. THE PARITY CHECK TRANSFORMATION ALGORITHM

We now summarize the PTA algorithm [9] to establish notation. Consider an (n,k) *RS* code with a parity check matrix H in the field GF(2^p). Let c be a codeword of length n. The symbols of the codeword c are mapped onto signals based on a selected modulation scheme and then transmitted through an AWGN channel. At the output of the channel a received vector r is obtained. Based on the vector r a reliability matrix R can be constructed. The matrix R is then fed into the PTA decoder.

The steps involved in one iteration of the PTA algorithm are as follows

1. *Getting the symbol reliability*: Find the highest values in each column of the R matrix. From these values, let the k highest values represent the most reliable symbols. The indices of these symbols are denoted by $\mathcal{K}$. The remaining $n-k$ values represent the least reliable symbols and their indices are denoted by $\mathcal{U}$.
2. *The H matrix transformation step*: Transform the H matrix into matrix H^t by performing row operations similar to Gaussian such that H^t is in a rearranged systematic form based on the indices $\mathcal{U}$ and $\mathcal{K}$. The transformation is done in such a way that the indices of $\mathcal{U}$ match the partitioned identity matrix and the $\mathcal{K}$ indices match the parity partition as shown in [9]. A

computationally efficient way of doing this is shown in [10].

3. *Performing the syndrome checks*: For $1 \leq i \leq (n-k)$, the i^{th} row of the matrix H^t can be denoted as H_i^t. A syndrome check is now performed using all the $n-k$ rows of the matrix H by performing hard decision detection on the R matrix to obtain a vector $\hat{r}$, and getting the dot product $\hat{r} \cdot H_i^t$. Due to the rearranged systematic structure of H_i^t, only one symbol with the index in $\mathcal{U}$ participates in the syndrome check. All the k symbols in $\mathcal{K}$ participate in the dot product.

4. *The correction step*: If the dot product is not zero, we decrease the symbol indexed in $\mathcal{U}$ by the value of a correction factor, δ, and decrease the symbols indexed in $\mathcal{K}$ by $\delta/2$. If the syndrome check is satisfied we add the δ to the symbol indexed in $\mathcal{U}$ and $\delta/2$ to the symbols indexed in $\mathcal{K}$.

5. *The update step*: These corrected reliabilities are then used to update the R matrix based on the $\mathcal{U}$ and $\mathcal{K}$ indices. The updated R matrix is then used in the next iteration.

6. *The stopping criterion*: steps 1 to 5 are repeated until all the $(n-k)$ syndrome checks are satisfied, or until a negative value appears in the matrix R.

From [9] it was shown that a smaller correction factor (δ) improves the performance of the algorithm. This, however, comes at the cost of increased number of iterations as the algorithm has to perform more corrections to the received codeword.

3. MODIFICATIONS TO THE PTA ALGORITHM

We now analyze the performance of the PTA and the effect of the modifications to the algorithm. Simulations are based on a (15,7) Reed-Solomon code using BPSK modulation in an AWGN channel. The value of δ used is 0.001.

3.1 Performance of the PTA based on the number of iterations

To better understand how the PTA algorithm works, the early stopping condition used in [9] is not considered. The only stopping criterion for the algorithm is when all syndrome checks are satisfied. This version of the PTA defined by the syndrome check as the only stopping condition is denoted as PTA$^{\gamma}$.
Table. 1 shows the results for simulations run for the PTA$^{\gamma}$ with 1000 codewords at an SNR of 0 dB. The number of codewords with error and the number of iterations required to satisfy the checks are recorded.

Fig. 1 shows simulations for the Hamming distance between the actual codeword and the decoded codeword at the output of each iteration of the PTA$^{\gamma}$. Results in Fig. 1 are representative for the 4 types of codewords decoded using the PTA$^{\gamma}$ in Table 1. The 4 types of codewords represented include: the codewords correctly decoded within 1000 iterations, the codewords decoded correctly with more than 1000 iterations, the codewords decoded incorrectly within 1000 iterations and the codewords decoded incorrectly for over 1000 iterations.

Table 1: Number of errors compared to the number of iterations for 1000 codewords

Number of iterations	detected codeword	Number of codewords
Less than 1000	Correct	853
	Wrong	54
More or equal to 1000	Correct	3
	Wrong	90

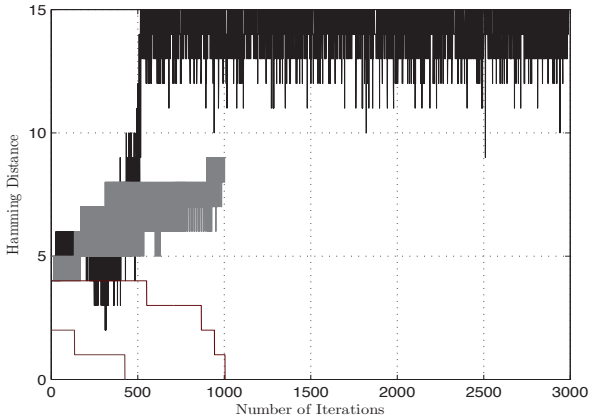


Figure 1: Comparing the Hamming distance to the Number of Iterations.

From Table 1 and Fig. 1 it can be seen that the PTA$^{\gamma}$ algorithm outputs a codeword, regardless if it is correct or incorrect, when it satisfies the syndrome checks. What this means is that more iterations for the PTA$^{\gamma}$ algorithm don't necessarily mean an improved performance with the algorithm. This can be seen especially when the algorithm runs for more than 1000 iterations. From Table 1 it can be seen that most of the syndrome checks for the correct codewords are also satisfied whenever the PTA$^{\gamma}$ runs less than 1000 iterations. Most incorrect codewords are received from the PTA$^{\gamma}$ whenever the algorithm runs for more than 1000 iterations.
From Table 1 only 3 codewords that run for 1000 or more iterations with the PTA$^{\gamma}$ are decoded correctly. This indicates the presence of a threshold in the PTA$^{\gamma}$ which occurs when the algorithm runs for more than 1000 iterations. Fig. 2 investigates the effect of different thresholds on the PTA$^{\gamma}$ by setting different maximum number of iterations (I_{max}) the algorithm can run.

From Fig. 2 it can be seen that the threshold of the PTA$^{\gamma}$ is at I_{max} = 1000 and that it serves as a point of saturation for the algorithm, as the performance appears to remain the same beyond this point. Thus, a set maximum value

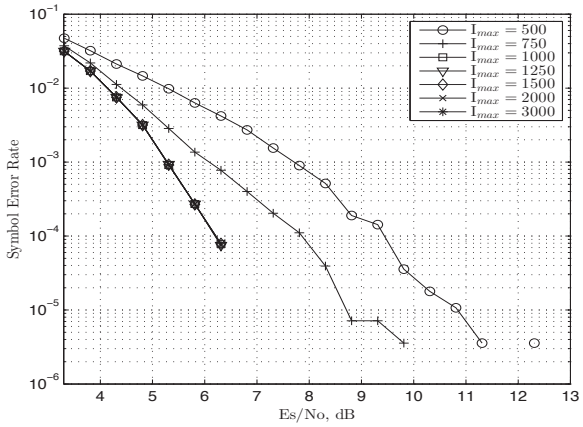


Figure 2: Performance comparison of different values of I_{max}

of 1000 iterations for the PTA$^{\gamma}$ should be used to prevent redundancy.

3.2 *Performance of the PTA based on the number of negative values in R*

A possible reason for the increased errors with more iterations could be the appearance of negative values formed in the reliability matrix, originating from the corrections done during each iteration. Simulations to see how the number of negative values in the reliability matrix corresponded to the actual codeword matching the received codeword at the output of the PTA$^{\gamma}$. The test was run for 1000 codewords. The results of these simulations were recorded in Table. 2.

From Table. 2, it can be seen that for most cases, the

Table 2: Number of errors compared to the number of negative values for 1000 codewords

Reliability Matrix	detected codeword	Number of codewords
Negative found	Correct	7
	Wrong	133
Remains Positive	Correct	858
	Wrong	2

presence of a negative value in the reliability matrix directly affect the number of errors of the received codeword at the output of PTA$^{\gamma}$. This result validates the early stopping condition of the PTA algorithm used in [9]. To prevent errors caused by the negative values, absolute values of the corrected reliabilites are used after each iteration of the PTA$^{\gamma}$. This modification of the PTA$^{\gamma}$ with absolute values is referred to as the absolute PTA$^{\gamma}$ and denoted as aPTA$^{\gamma}$.

3.3 *Performance of the PTA based on the Stagnant check.*

If the absolute values are to be used, the early stopping condition defined in [9] is not applicable as the reliability matrix does not run into a negative value. To prevent the aPTA$^{\gamma}$ from running upto I_{max} iterations in the event it is unable to find the correct codeword, a new early stopping condition is required. A modification of the stagnant check [11], is added to the algorithm to perform this function. The stagnant check acts as a predictive algorithm, by trying to determine if the algorithm will have a decoding failure or a decoding success.
The stagnant check algorithm works as follows

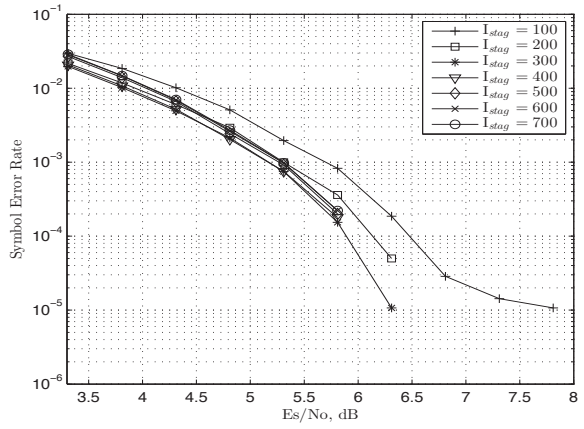
1. At a given iteration I_{α}, the weight of the unsatisfied syndrome checks ($w(s)$) is noted.
2. The value of $w(s)$ is noted for each iteration after I_{α} until a specified iteration I_{stag} is reached.
3. At iteration I_{stag}, a stagnant check is done.
    - If $w(s)$ is the same from I_{α} to I_{stag} then the algorithm is perceived to be stagnant (unable to find the correct codeword), and the decoding process is stopped.
    - If $w(s)$ has changed from I_{α} to I_{stag} then the aPTA$^{\gamma}$ runs until all the syndrome checks are satisfied, or until I_{max} is reached.

The main aim of the stagnant check is to help reduce the number of iterations required by the aPTA$^{\gamma}$. To get an optimum performance of the aPTA$^{\gamma}$ with the stagnant check, simulations are done for different values of I_{stag} and run for $I_{max} = 1000$. Simulations are run for $I_{\alpha} = 1$ and the stagnant check was done at $I_{stag} = 100$, $I_{stag} = 200$, $I_{stag} = 300$, $I_{stag} = 400$, $I_{stag} = 500$, $I_{stag} = 600$, $I_{stag} = 700$. The average number of iterations run by each was noted. The results for these simulations can be seen in Fig. 3.

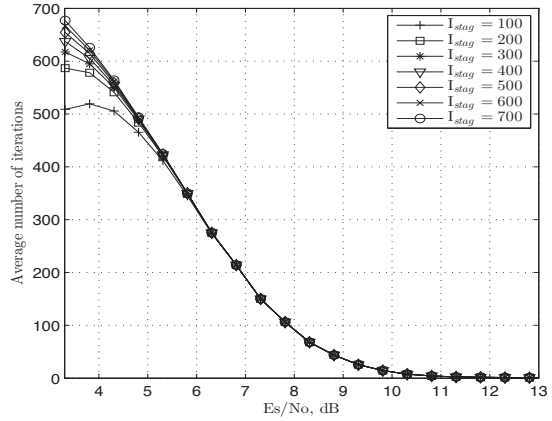
From Fig. 3 it can be seen that the aPTA$^{\gamma}$ with the value of $I_{stag} = 400$ gives the best performance when compared to the rest. The aPTA$^{\gamma}$ with the stagnant check is referred to as the Modified Parity check Transformation Algorithm (MPTA).

3.4 *Performance of the PTA based on the value of the correction factor, δ*

From Fig. 3(b), it can be seen that even with the stagnant check the algorithm still runs for many iterations in low SNR regions. The main reason for this is the use of a small value of δ. The smaller the value of δ the better the perfomance, but this is at the cost of an increased number of iterations as shown in [9]. This is because there is not a large difference in the corrections made by δ in each iteration for the wrong symbols as it attempts to satisfy the syndrome checks. Since the difference in the corrections made by a δ of 0.001 are quite small several iterations would be required to satisfy the checks. Simulations for different values of δ with the aPTA$^{\gamma}$ are done to test for the performance and the average number of iteration required by the algorithm. No stagnant check is used because an accurate representation of the average number of iterations

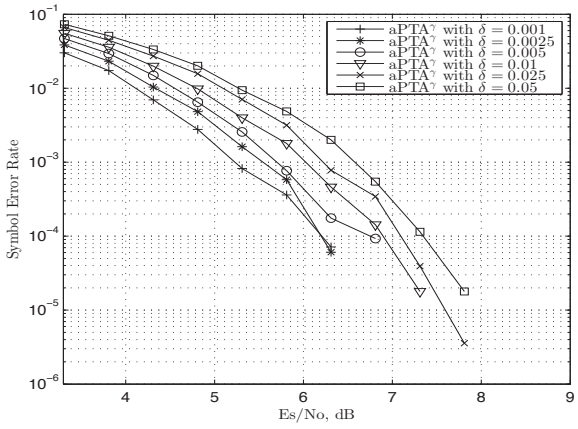


(a) SER Perfomance for different values of I_{stag} for the MPTA

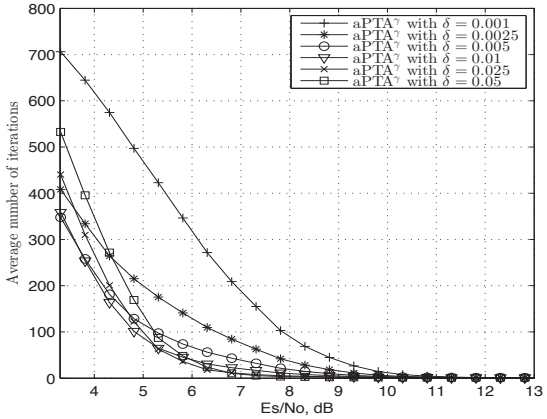


(b) Average number of iterations for the MPTA

Figure 3: Perfomance of the MPTA based on the value of I_{stag}



(a) SER Performance of different aPTA$^\gamma$ with different values of δ



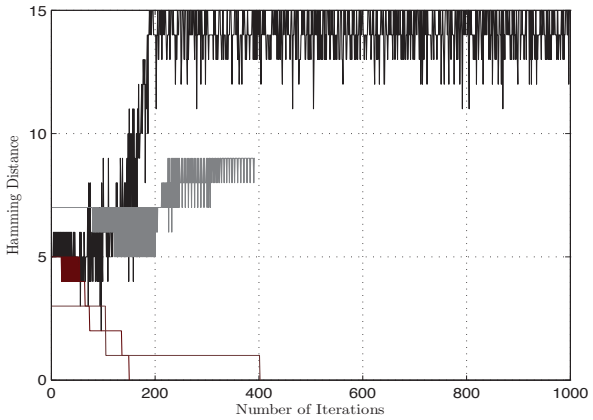
(b) Average number of iterations for the aPTA$^\gamma$ with different values of δ

Figure 4: Perfomance of the aPTA$^\gamma$ based on different values of δ

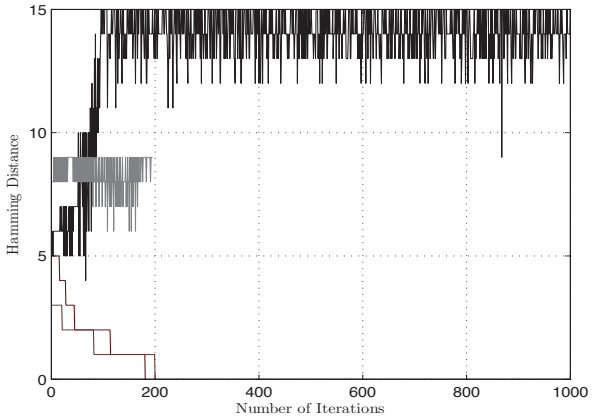
run by the algorithm for each SNR is required. The results for these simulations can be seen in Fig. 4.

Fig. 4 validates the results shown in [9] with a BSPK modulation scheme for the PTA. It can also be seen that the number of iterations run by the aPTA$^\gamma$ between $\delta = 0.005$ and $\delta = 0.001$, increases as the value of δ reduces for lower SNR regions. However, the opposite seems to happen between $\delta = 0.01$ and $\delta = 0.05$. This is due to these values of δ making a large difference in the corrections made to the soft information. This causes the algorithm to change the reliability of the symbols faster, thus passing the correct symbols as it satisfies the checks. It is evident from Fig. 4 that the value of the correction factor should be $\delta < 0.01$ for better SER results to be obtained with the algorithm.
To reduce the number of iterations run by the MPTA, a discreet variable δ approach is added to the algorithm. For this implementation, two scenarios are considered. A case of increasing values of δ, and a case of reducing values of δ. In both cases, the value of δ changes with respect to the number of iterations.
For this analysis, three values of δ are used. The values of δ chosen are $\delta = 0.005$, $\delta = 0.0025$ and $\delta = 0.001$. The reason these values of δ have been selected is because the performance difference between $\delta = 0.001$ and $\delta = 0.005$, from Fig. 4, is about 0.5 dB.
To help with the implementation of this form of discreet variable δs with the algorithm, a similar simulation to the one done in Fig. 1 is done for the PTA$^\gamma$ with $\delta = 0.005$ and $\delta = 0.0025$ for 1000 codewords. This is done to help with the assignment of the number of iterations that each δ receives. The results for these simulations can be seen in Fig. 5, Table 3 and Table 4.
The simulations are let to run for as many iterations until the syndrome checks are satisfied. For Fig. 5, to better see the results, only the first 1000 iterations are shown. Once again, results for only 4 codewords that are representative of most of the other codewords decoded with the PTA$^\gamma$ are used. The 4 types of codewords are highlighhted in the results recorded in Table 3 and Table 4.

From Fig. 5 and Table 4 it can be seen that for $\delta = 0.005$ most of the correct received codewords are found within 200 iterations. Beyond this, the algorithm begins to saturate and is unable to find the correct codeword to satisfy the syndrome checks. For $\delta = 0.0025$ the algorithm



(a) Comparing the Hamming distance to the Number of iterations for $\delta = 0.0025$



(b) Comparing the Hamming distance to the Number of iterations for $\delta = 0.005$

Figure 5: Performance of the PTA$^{\gamma}$ with $\delta = 0.0025$ and $\delta = 0.005$ based on the number of iterations

Table 3: Number of errors compared to the number of iterations for 1000 codewords with $\delta = 0.0025$

Number of iterations	detected codeword	Number of codewords
Less than 400	Correct	808
	Wrong	36
More or equal to 400	Correct	14
	Wrong	142

Table 4: Number of errors compared to the number of iterations for 1000 codewords with $\delta = 0.005$

Number of iterations	detected codeword	Number of codewords
Less than 200	Correct	733
	Wrong	22
More or equal to 200	Correct	24
	Wrong	221

appears to saturate after about 400 iterations as seen in Fig. 5 and Table 3. Therefore, of the 1000 maximum iterations for the MPTA, the number of iterations each δ runs is assigned with respect to the SER perfomance shown in Fig. 4(a) and the performance based on the number of iterations required to satisfy the checks shown in Fig. 1 and Fig. 5. For the case of the increasing δ, the number of iterations is split as follows

- $\delta = 0.001$ runs for the first 625 iterations
- $\delta = 0.0025$ runs the next 300 iterations
- $\delta = 0.005$ runs the last 75 iterations

For the case of the decreasing δ, the number of iterations is split as follows

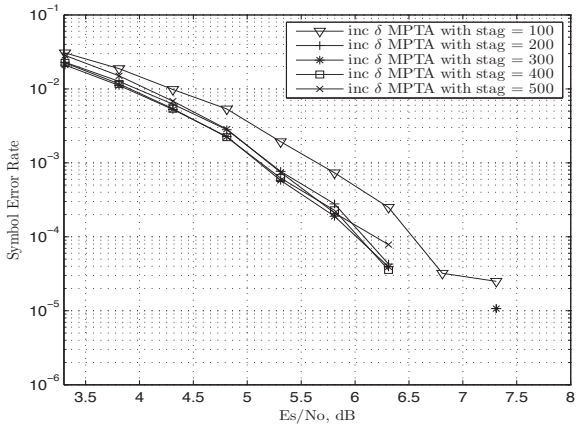
- $\delta = 0.005$ runs for the first 75 iterations
- $\delta = 0.0025$ runs the next 300 iterations
- $\delta = 0.001$ runs the last 625 iterations

Simulations for the discreet variable δ version of the MPTA are done to test for the optimum performance with different values of I_{stag}. These simulations are for SER performance and the average number of iterations required by the algorithm. The values of I_{stag} used in the simulations for the decreasing δ are smaller than those used for increasing δ. The reason for this that for the decreasing δ case, the first value of δ used is 0.005. An earlier stagnant check for $\delta = 0.005$ is required as the corrections it makes to the codeword during each iteration are larger than those of $\delta = 0.001$. As a result it runs into a stagnant state much earlier as shown in Fig. 5. The results of these simulations for the both cases of increasing and decreasing δ can be seen in Fig. 6 and Fig. 7 respectively.

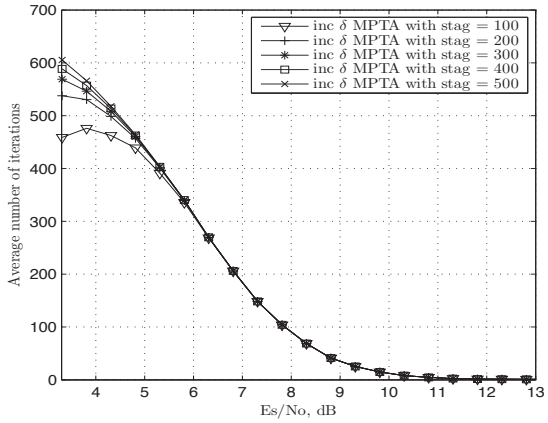
From Fig. 6 it can be seen that the best performance, in terms of SER, is obtained when $I_{stag} = 400$. It is naturally outperformed by $I_{stag} = 100$, $I_{stag} = 200$ and $I_{stag} = 300$ in terms of the number of iterations required for the lower SNR values. Based on the SER performance, the value of $I_{stag} = 400$ was selected for the increasing δ version of the MPTA in the comparative study.
A similar observation can be done in Fig. 7 with $I_{stag} = 80$, as it the gives best performance in terms of SER. In terms of the number of iterations, it is outperformed by $I_{stag} = 20$, $I_{stag} = 40$ and $I_{stag} = 60$ for low SNR values. Based on the SER performance, the value of $I_{stag} = 80$ was selected for the decreasing δ version of the MPTA in the comparative study.

4. PERFORMANCE ANALYSIS

Fig. 8 shows simulations for the performance comparison of PTA to that of the MPTA with a single δ of 0.001 and $I_{stag} = 400$, an increasing δ with $I_{stag} = 400$ and a decreasing δ with $I_{stag} = 80$.
From Fig. 8 it can be seen that the single δ MPTA and the increasing δ MPTA have an almost identical performance and they both outperform the PTA in terms of SER. In



(a) SER Perfomance for Increasing δ MPTA with different values of I_{stag}



(b) Average number of iterations for the increasing δ MPTA for different values of I_{stag}

Figure 6: Performance of the MPTA

terms of the average number of iterations for low SNR areas, the decreasing δ MPTA significantly outperforms all versions of the PTA. However, this is at a cost of about 0.5 dB. This SER performance difference justifies the use of the decreasing δ MPTA when a trade-off between SER performance and number of iterations is required. The increasing δ MPTA runs for less iterations than the PTA and gives a better performance. The single δ MPTA gives a better perfomance than the PTA but gives no difference in the average number of iterations.

5. CONCLUSION

In this paper, we are able to develop three different versions of the MPTA, each with its own trade-offs. The single δ MPTA increases the performance of the algorithm but at no reduction in the number of iterations. The increasing δ MPTA outperforms the PTA in terms of both the SER and the number of iterations required to decode. It also gives an almost identical performance to that of the single δ MPTA while running for less iterations in the low SNR regions. Finally, the decreasing δ MPTA significantly reduces the average number of iterations run by the algorithm by well over 400 iterations. This reduction in the number of iterations comes at the cost of a loss of less than 0.5 dB when compared to the PTA.

ACKNOWLEDGEMENT

The financial assistance of the National Research Foundation (NRF) of South Africa towards this research is hereby acknowledged. Opinions expressed and conclusions arrived at, are those of the authors and are not necessarily to be attributed to the NRF. The financial support of the Centre for Telecommunication Access and Services (CeTAS), the University of the Witwatersrand, Johannesburg, South Africa is also acknowledged.

REFERENCES

[1] I. S. Reed and G. Solomon, "Polynomial Codes over Certain Finite Fields," *J. Soc.Ind. Appl. Maths.*, 1960.

[2] J. Massey, "Shift-register synthesis and BCH decoding," *Information Theory, IEEE Transactions*, 1969.

[3] E. R. Berlekamp, "Algebraic Coding Theory," *New York: McGraw-Hill*, 1968.

[4] S. H. Y. Sugiyama, M. Kasahara and T. Namekawa, "A method for solving key equation for decoding goppa codes," *Information and Control*, 1975.

[5] L. R. Welch and E. R. Berlekamp, "Error correction for algebraic block codes," *Patent US 4 633 470*, 1986.

[6] R. Koetter and A. Vardy, "Algebraic Soft-Decision Decoding of Reed-Solomon Codes," *Information Theory, IEEE Transactions on*, 2003.

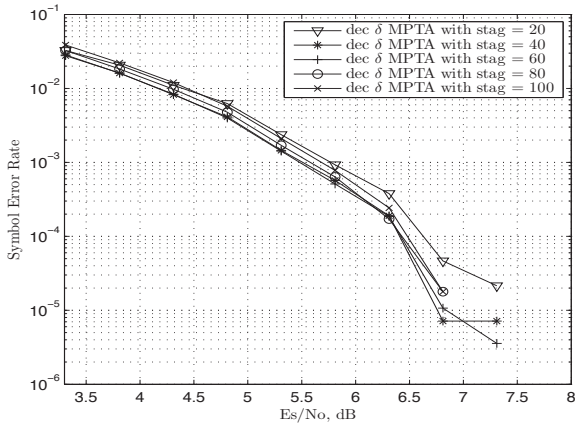
[7] V. Guruswami and M. Sudan, "Improved decoding of Reed-Solomon and Algebraic-Geometry Codes," *Information Theory, IEEE Transactions on*, 1999.

[8] J. Jiang and K. Narayanan, "Iterative Soft-Input Soft-Output Decoding of Reed Solomon Codes by Adapting the Parity-Check Matrix," *Information Theory, IEEE Transactions on*, 2006.

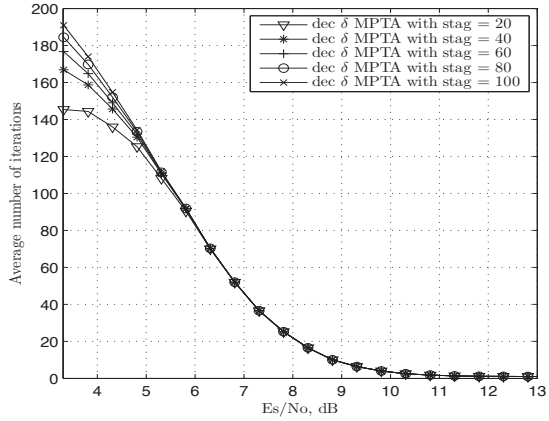
[9] O. Ogundile, Y. Genga, and D. Versfeld, "Symbol level iterative soft decision decoder for Reed-Solomon codes based on parity-check equations," *Electronics Letters*, vol. 51, no. 17, pp. 1332–1333, Aug. 2015.

[10] D. Versfeld, J. Ridley, H. Ferreira, and A. Helberg, "On Systematic Generator Matrices Reed-Solomon codes," *Information Theory, IEEE Transactions on*, vol. 56, no. 6, pp. 2549–2550, June 2010.

[11] B. Shin, S. H. Kim, J. S. No, and D. J. Shin, "New stopping criteria for decoding LDPC codes in H-ARQ systems," in *Information Theory and Its Applications, 2008. ISITA 2008. International Symposium on*, Dec 2008, pp. 1–5.

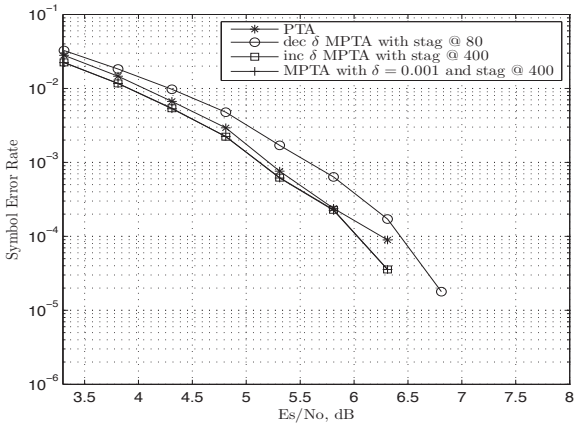


(a) SER Perfomance for decreasing δ MPTA with different values of I_{stag}

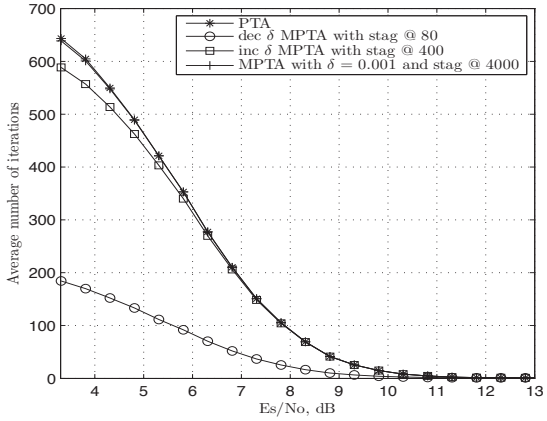


(b) Average number of iterations for the decreasing δ MPTA for different values of I_{stag}

Figure 7: Performance of the MPTA



(a) SER Perfomance for the MPTA and the PTA



(b) Average number of iterations for the MPTA and the PTA

Figure 8: Performance of the MPTA compared to the PTA

A TECHNICAL AND ECONOMIC COMPARISON BETWEEN TRADITIONALLY EMPLOYED AND EMERGING FAULT LEVEL MANAGEMENT SOLUTIONS AT DISTRIBUTION VOLTAGES.

M.F. Khan*, A.L.L. Jarvis *, E.A. Young **, R.G. Stephen***

** School of Electrical, Electronic and Computer Engineering, University of KwaZulu-Natal, Durban, 4041, South Africa. E-mail: KhanMa@eskom.co.za and Jarvis@ukzn.ac.za*
*** Institute of Cryogenics, Engineering Sciences, University of Southampton, United Kingdom. E-mail: E.A.Young@soton.ac.uk*
**** Technology, Eskom Holdings Pty Ltd. E-mail: StephRG@eskom.co.za*

Abstract: Network fault levels are reported to be increasing and this is often attributed to an increase in network interconnectivity and localised generation. When the fault level at a substation increases beyond the rated value of the installed equipment, a power utility traditionally responded by either (i) replacing the equipment with higher rated equipment or, (ii) installing series reactors or, (iii) replacing the existing transformers with high impedance transformers. Using a South African case study, this paper compares both the effectiveness and financial viability of a superconducting fault current limiter (SFCL) against the traditional three options. When one also considers the operational or 'energy' cost associated with all these options it was found that a high capital cost was sometimes offset by lower energy costs over a 25 year service life. Regional prices of electricity and tariffs therefore have a significant impact on a utility's choice of fault management solutions.

Key words: fault level management, power system management, superconducting fault current limiters.

1. INTRODUCTION

A high fault level is not intrinsically undesirable as it is an indication of the strength and robustness of a power system, but it becomes so when it is larger than the rating of the installed equipment. It is often cited that bus-bar fault levels on power grids are continually increasing [1], [2]. This then requires an intervention to mitigate against the inherent operational and safety risks.

Fault levels are increasing, primarily due to network interconnectivity, in an effort to improve power delivery reliability, and an increase in generation to meet the demands of increasing growth [3]. Government and utility initiatives have also resulted in an increase in the number of independent power producers, co-generation schemes and micro-renewable projects and this is known to increase the local generating capacity of the network and thus the fault levels [4].

Current research towards the development of superconducting fault current limiters (SFCL) for large scale power grid applications has led to the establishment of long term pilot installations on existing power grids and test grids to prove operability and performance, for example, the recent installations at San Juan de Dios Substation in Mallorca (Spain) [5], and Icheon substation (Korea) [6]. These installations are testimony that SFCLs are now evolving to a position wherein it too may be considered as an effective means of fault level management. This is evident even in the developing world, for example, a recent study on the impact of SFCL inclusion to the Abu Dhabi 132 kV network [7].

Eskom is one of the largest power utilities in the world and generates 95% of the electricity used in South Africa (nominal capacity of 41 995 MW) [8]. It is also responsible for the South African national grid. The authors conducted a comparison between the current network fault levels and the installed switchgear at all of the substations on Eskom's distribution network and discovered that there were 82 substations wherein the busbar fault level exceeds the installed network circuit breaker ratings. Although this represents only a small component of Eskom's installed base (2.52%), measures have already been put in place to manage this and the future risk associated with continually increasing busbar fault levels. SFCLs were not amongst the mitigation technologies considered as it was considered to be too expensive and complex an option.

South Africa also experienced a major energy crisis in 2008 when the ever increasing demand for electricity was unable to be met by the existing installed generation plants. They responded by launching a number of initiatives to promote large scale renewable energy development. The Renewable Energy Bids (REBID) process [9], wherein a ceiling tariff rate is set for each technology and interested parties bid for power purchase agreements, was the most successful of these initiatives.

The impact of localized renewable energy generation on distribution network fault levels has yet to be sufficiently researched owing largely to variations of their geographic

location and size. The connection of generation sources in distribution networks, which were originally planned and designed to supply radial loads, would have a considerable impact on bus-bar fault levels [4].

This paper utilizes a network case study to investigate the impact of increased renewable generation on fault levels and by extension, its impact on installed circuit breaker ratings exceedance and any associated energy loss. The South African Distribution Network Code [10] states in Section 7.2.1(3) that when making an investment in the power network the following criteria must apply:

"…the need to invest must first be decided on technical grounds. All investments must be the least life-cycle cost technically acceptable solution…".

The contribution of this paper is to therefore confirm the technical suitability of the fault management options considered by power utilities today and to present a realistic life cycle financial comparison of SFCL's with existing solutions. This in turn, highlights the significance of the regional cost of electricity when determining which fault level management tool is most effective.

2. FAULT CURRENT MITIGATION OPTIONS

We focus on four fault current mitigation solutions. The option of network reconfiguration, for example, the action of operating with the MV bus-bar split was not considered. Although it is known that this would reduce the fault level and come at a zero cost, it would also result in a loss of network reliability and flexibility, which is an undesirable consequence for a power utility.

2.1 Air core reactor

The series connected air core reactor represents the traditional option for fault current management in a power network. It addresses the fault level problem by adding impedance to the network. It is a passive device that requires minimal maintenance, has a relatively small physical footprint and is available at a cost that is significantly lower than any of the other options considered. It is however continuously connected and therefore consumes a significant amount of electrical power. The associated volt drop is compensated for by on-load transformer tap changers that regulate the voltage on the MV busbar.

2.2 High impedance transformer

Standard power transformers on a conventional electrical grid are specified with a typical impedance of 8%. High impedance transformers, with an impedance that ranges between 17% and 20%, have been introduced by power utilities as a fault level management measure. This passive mitigation measure operates on the same electrical principle as an air core reactor and therefore shares many of its advantages and disadvantages. An advantage when compared to an air core reactor is that it requires no additional space in an electrical yard and is therefore an ideal option when a retrofit solution is required with limited additional space available.

When considered as a solution to lower the fault level due to the availability of localized generation on the MV bus-bar, the losses are not higher, as the energy loss is a function of the load current that passes through the transformer, and that load current is reduced when generation is introduced directly onto the MV bus-bar. High impedance transformers are understandably more costly but these are however available to Eskom via long term contracts at a small premium when compared to the price of a standard transformer for the various voltage options. It is therefore an ideal option for new installations where it is perceived that fault levels are, or will become, a concern. When utilizing this option however, a power utility must also consider the additional costs associated with increased strategic spares holding.

2.3 Equipment "up-rating"/ upgrade

As discussed above, high fault levels are not necessarily undesirable, so long as the fault level is below the design limits of the installed substation equipment. One of the options available to utilities is to therefore replace the installed equipment with equipment that has a higher short circuit withstand capacity. Of the equipment installed in a substation, the one that is typically found with the lowest short circuit withstand capacity is the installed switchgear.

The replacement of installed switchgear in a substation is a costly and time-consuming option. The existing equipment would need to be decommissioned and removed before the new equipment can be installed and commissioned and this requires an extended outage. This option is, however, ideally suited to identified substations where the installed equipment has passed or is nearing the end of its service life. The choice of merely replacing the equipment in a substation yard when it is identified that the fault level has increased beyond the equipment rating is also not always practical. For example, substation components like the substation earth-mat, would have been designed for a particular fault level, and would have to be strengthened to ensure compliance viz. touch and step potentials [11]. The significant advantages to the equipment uprating option are that there is no additional maintenance requirement or operation (energy loss) costs.

2.4 Superconducting fault current limiter

Recent installations of resistive superconducting fault current limiters on power grids has propelled this technology from the laboratory into a potentially viable alternative for fault level management [5], [6]. The device operates by allowing load current to pass through superconductor tape/wire that have been cooled to below a critical temperature thereby presenting minimal additional resistance. When a fault is introduced, the current increases above a threshold value which causes the superconductor to change phase and introduce resistance into the system, within the first half cycle, thereby 'instantaneously' reducing the fault current.

The SFCL is either connected on the MV bus-bar as a replacement to the existing bus section circuit breaker or in series with the incoming feeder. When a SFCL replaces an existing bus-section circuit breaker, it results in reduced operational flexibility. To overcome this, it is recommended that instead of replacing a bus section circuit breaker, a SFCL should be installed in series with one.

It is often stated that a SFCL is a zero energy loss solution, but this is not an entirely accurate reflection. Although, the SFCL dissipates minimal energy during normal operation due to the inherent resistive characteristics of superconductors, there still remains an energy requirement for this option. This is primarily for the SFCL cooling requirements and this energy loss is therefore independent of load current.

Other considerations need to be accounted for before installing a SFCL onto a power grid as its impact is not only limited to fault level management. SFCLs can influence power system stability [12] and substation reliability [13].

3. CASE STUDY

A network case study was selected as a way to compare the effectiveness of the various fault level management options. The criteria used to select the substation for the case study were:

- One wherein the existing fault level was between 90 – 100 % of the installed equipment rating
- That it be situated in an area with the potential for localized generation projects
- Enough space installed or adjoining to it that could accommodate all fault management options considered, and
- Located within reasonable proximity to allow site visits to confirm equipment ratings etc.

The '90% – 100%' fault level criterion was selected to verify the potential impact that localized generation could have at substations where the circuit breaker ratings have not been exceeded as yet. The effectiveness of the different fault level mitigation options in response to the renewable energy technologies identified could also be assessed. The justification for the criteria regarding the location of the substation, is that there is an increased probability of localized generation when there are no space restrictions as would typically be found in an urban environment. A substation that met all the listed criteria was identified and selected. Figure 1 below is the single line diagram for the selected substation.

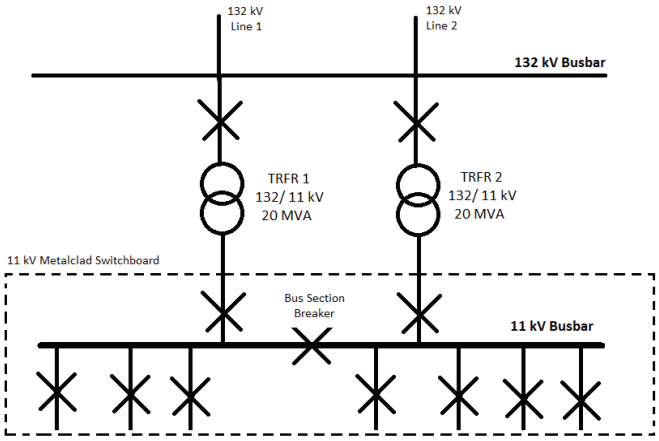


Figure 1: Operating diagram of the selected substation

3.1 The impact of increased localized generation

The network impact studies for the introduction of localized renewable energy generation was determined by considering projects where successful power purchase agreements have been concluded and is representative of installed capacity in megawatts (MW). This was considered to be a realistic means of determining the 'typical' sizes for the various types of renewable projects. An analysis of the REBID data from 2012 to 2014 is summarized in Table 1.

Table 1
Consolidated REBID Data (2012 -2014)

	Wind	**PV**	**Small projects**	**Small Hydro**
Maximum (MW)	140.0	75.0	5.0	6.2
Minimum (MW)	20.6	5.0	1.0	1.2
Average (MW)	90.0	45.7	4.7	2.8
Median (MW)	77.2	32.9	5.0	2.4

The median for wind projects is 77.2 MW and is therefore not considered for this study as a project of this magnitude would always be introduced on the HV busbar, and this study focuses on embedded generation projects on the MV busbar. There was only one

hydroelectric and one biomass power purchase agreement for the period analysed. As both technologies would have utilized synchronous generation, only biomass, being the larger of the two with a capacity of 16 MW was considered in the simulation below. The majority of projects in the 'small projects' category represented photovoltaic projects and were therefore modelled as such.

3.2 Fault Level Simulations

Simulation and analysis software, DIgSILENT PowerFactory™ was used to model the substation and the impact that various renewable energy projects could have on its existing busbar fault level rating. The median capacity for the various renewable technologies, as indicated in Table I, was simulated to observe the impact that a typical generation in-feed could potentially have on the existing fault level at the substation busbar. It was assumed for the purpose of these simulations that the system fault occurred at the substation MV bus-bar. The circuit breakers presently installed at the substation chosen for the case study has a fault level rating of 18.4 kA.

The machine parameters (e.g. source impedance, sub transient reactance etc.) used for the different renewable generators simulated in this study were as obtained from the DIgSILENT™ library. All models contained within this library use parameters as obtained from manufacturers so that load flow studies that are conducted provide realistic results. Synchronous generators were modelled for hydroelectric schemes and the biomass scheme as they are traditionally favoured over asynchronous generators for large capacity machines. The invertor associated with photovoltaic power generation is modelled within the 'Photovoltaic Generator' element (Figure 2) and was modelled with a power factor of 0.95.

No simulations are obviously required to confirm the effectiveness of 'up-rating' the installed switchgear. For this study an 11 kV air core reactor with a rated inductance of 3.05 mH per phase was selected as similarly specified units are currently utilized elsewhere on the network. Standardization was preferred to both reduce costs and minimize strategic spares holding. The high impedance transformer was simulated with an impedance of 20%. The SFCL was not simulated as it has been shown to effectively limit the fault current of this magnitude and also has negligible system losses during normal operation [5], [6].

It was also noticed in the simulations that the utilization of the series air core reactor and the high impedance transformer had a negligible effect on the nominal tap position of the installed power transformers. Utilisation of these methods was therefore found to have a negligible effect on network voltage regulation.

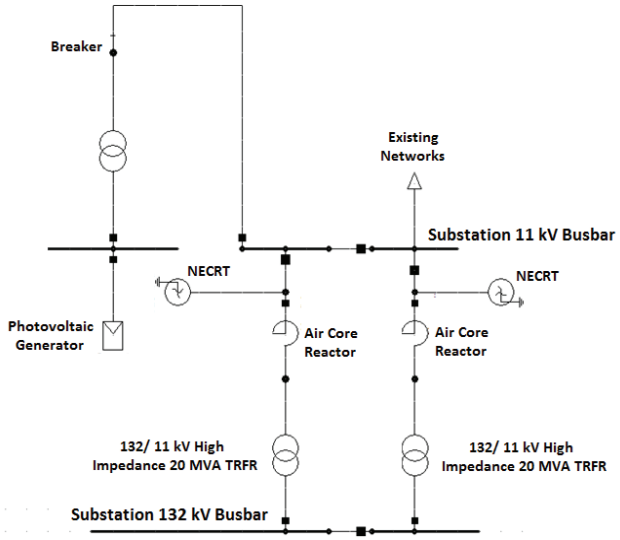


Figure 2: DIgSILENT™ models for a Photovoltaic Project with installed series air core reactors

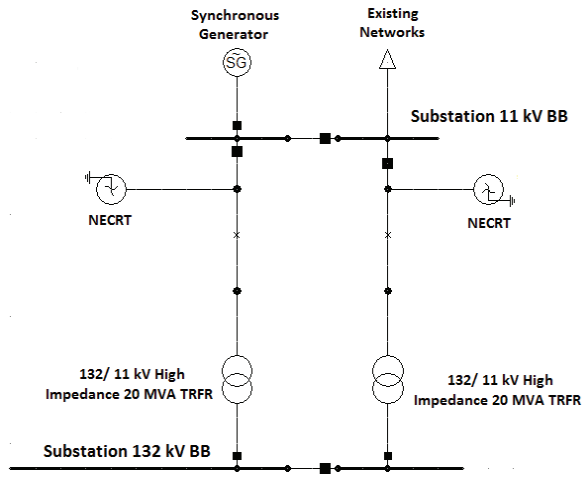


Figure 3: DIgSILENT™ models for a Synchronous generator utilizing a high impedance transformer

Table 2 summarises the impact on the simulated short circuit fault level when various renewable technologies are introduced to the local network. It also illustrates the effectiveness of the specified series reactor and the high impedance transformer as an effective fault level management device.

An analysis of Table 2 indicates that with the exception of the 5 MW photovoltaic in-feed, all other simulations indicate that the circuit breaker rating would be exceeded for the various renewable technologies considered and an intervention would therefore be required to ensure operational safety.

Table 2: Impact of renewable energy projects and mitigation options on busbar fault level

		3 phase I_{SC} (kA)	I_{SC} as a % of Circuit breaker Rating
Existing Installation		**17.8**	**96.97%**
5 MW Hydro Generator (Synchronous Generator)	Impact on Fault level	19.4	105.4%
	Series Reactor	9.4	51.1%
	High Impedance Tx	11.4	62.0%
16 MW Biomass Generator (Synchronous Generator)	Impact on Fault level	24.1	131.0%
	Series Reactor	14	76.1%
	High Impedance Tx	16.1	87.5%
5 MW Photo-voltaic Plant (Inverter)	Impact on Fault level	18.1	98.4%
	Series Reactor	8.1	44.0%
	High Impedance Tx	10.1	54.9%
30 MW Photo-voltaic Plant (Inverter)	Impact on Fault level	19.6	106.5%
	Series Reactor	9.7	52.7%
	High Impedance Tx	11.8	64.1%

3.3 Energy Loss Calculations

The energy loss and cost associated with different fault current mitigation methods needs to be considered in order to determine the total life cycle cost.

The 'equipment upgrade' option would result in a zero energy loss and although a SFCL has negligible losses during normal operation, the energy required by the cryogenics require consideration. This was obtained by referencing the normal load current at the selected substation to the power loss associated with the design of an installed SFCL [5] i.e. the maximum cooling loss at room temperature was estimated to be 8500 W at typical network load current.

The energy loss associated with the use of a series core reactor and a high impedance transformer was simulated using DIgSILENT™. A typical daily load profile for this network (with morning and evening peaks) was modelled at the selected substation to determine the increase in energy loss when utilizing either an air core series reactor or a high impedance transformer for a day. This was then used to determine the annual operational (energy) cost. Table 3 shows the daily energy usage increase for the various fault management technologies identified over the installed installation.

Table 3: Daily energy requirements associated with the fault current mitigation methods identified

	Energy increase (kWh)
High Impedance Transformer	633.7
Air core series reactor	321.3
Equipment up-rate	0
Superconducting fault current limiter	204

The energy cost associated with the total lifecycle was determined by using existing energy prices with an assumed annual inflation rate of 6% p.a to more accurately determine the lifecycle cost over 25 years. Table 4 summarises the total lifecycle costs for the options considered in this study.

4. ANALYSIS OF FAULT LEVEL MANAGEMENT OPTIONS

A power utility must consider two critical aspects before adopting a fault level mitigation solution, the technical and the financial. The case study above shows that all options considered will either lower the fault level to within specified limits or increase the existing fault level rating of the installed equipment. The financial impact for choosing a fault level mitigation solution therefore remains as the other critical aspect that requires consideration. In doing so, it is prudent to not merely consider the initial capital cost but to rather evaluate the total lifecycle cost, which includes the costs associated with purchase, operation and maintenance. At Eskom, primary plant equipment at substations are designed to have a service life of 25 years [14].

Capital costs were obtained from recent purchase invoices or contracted purchase agreements with Eskom and suppliers, with the exception of the SFCL, which was the reported acquisition price for an SFCL recently

Table 4: Lifecycle costs for fault level management technologies investigated
(Based on an exchange rate of R 14.21/ Euro and R 10.60/ $)

	Series Reactor	**Switchgear upgrade**	**High Impedance Tx**	**SFCL**
Capital Cost	$ 160,239	$ 650,822	$ 1,494,645	$ 1,742,736
Energy Cost/ day	$15	$ 0	$29	$10
Energy Cost (p.a)	$ 5,509	$ 0	$ 10,865	$ 3,498
Energy Cost (25 years)	$ 302,238	$ 0	$ 596,128	$ 191,907
Total Lifecycle Cost	**$ 462,477**	**$ 650,822**	**$ 2,090,773**	**$ 1,934,643**

purchased by Western Power Distribution [15].

Maintenance costs were only a factor for an SFCL and it was assumed that maintenance would be undertaken on the cryo-cooler once a year. However, in the South African context this cost would be an assumption and it was therefore excluded from the case study with the understanding that the reader is aware that an additional undetermined maintenance cost is applicable to the SFCL whereas all other technologies evaluated would have a zero or negligible increase in maintenance costs.

Although the air core reactor has the lowest capital investment cost, it has a considerable energy cost with the high impedance transformer having the highest energy cost. Of all the options evaluated, the series reactor was found to be the most cost effective over a 25 year time period. The switchgear upgrade option was in this case study the next most cost effective option. As mentioned earlier, this study assumed that the earth-mat in the substation yard does not require uprating.

The installed circuit breakers at the selected substation were installed in 1978 and have therefore surpassed its service life of 25 years and are due for replacement. It therefore has a zero net asset value. Refurbishment of this substation would result in the circuit breakers being replaced, and the new circuit breakers on contract with Eskom are rated for a fault level of 25 kA [14]. The maximum simulated fault current in Table II is 24.1 kA. Therefore, for this specific case study it appears that the solution to the problem of circuit breaker exceedance would be best addressed by "uprating" the circuit breakers even though it appears to not be the most cost effective from a life cycle costing perspective.

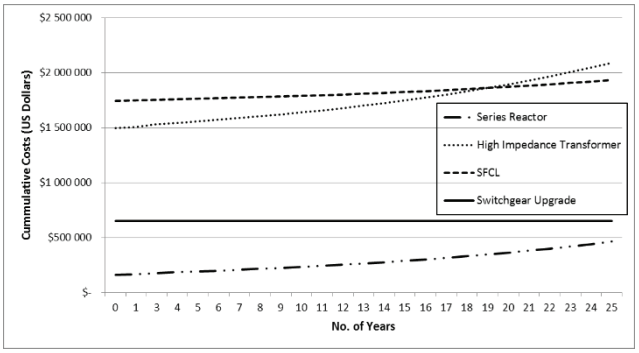


Figure 4: Accumulated cost of fault management options in South Africa. (Based on an exchange rate of R 14.21/ Euro and R 10.60/ $)

The cost of utilizing a high impedance transformer was found to be the most energy intensive option. When considering the high capital cost of the high impedance transformer, one must bear in mind that this solution combines a fault level management tool with an essential item of plant in the substation and that the true financial cost of this fault level exceedance solution is therefore the total cost of the project less the remaining asset value of the existing transformers. As these transformers were purchased and installed in 1998, the true financial cost of this option considering depreciation, purely as a means to reduce the existing fault level, is therefore $ 1,310,434 for the case study considered and is therefore financially not a viable solution in this instance. One should however also bear in mind that utilisisation of this option needs to be part of a much larger fault management philosophy as high impedance transformers would now be required to be purchased as part of the utility strategic spare fleet. Large-scale adoption of this philosophy could prove to be very expensive in the long term when factoring in the high energy cost of this option. It could however prove to be a viable option when building a new substation. The associated energy cost in this instance should be weighed against the increase in utilization of higher rated equipment.

Cooling costs for this study were determined using the calculated energy losses based on the 'Eccoflow' installation in Mallorca [5] which employs a closed cycle cooling system. Although an open cycle cooling system would utilize significantly less electrical energy, it would require increased specialized cryogenic maintenance and operation. The purchase price for a resistive SFCL was obtained from the recent procurement by Western Power Distribution (WPD) of two SFCLs to "future-proof" the Birmingham power distribution network [15]. This was the most recent cited example of a SFCL purchased to manage fault levels on a utility grid.

The very high initial capital investment cost for SFCLs remains the most significant factor in the high life-cycle cost determined for this option. It is understood that up to 3 km of high temperature superconductor (HTS) tape is utilized in the construction of a SFCL [5]. The cost of the HTS tape is known to be a significant factor in the overall capital cost of the SFCL. Tape prices are decreasing and will decrease even further with improved market penetration. The operating energy cost of the cryo-cooler was found to be comparable with that of the air core reactor however, it is clear to see that significant reductions in cryo-cooler efficiencies will still not affect the life cycle costs substantially.

For SFCLs to be viable for power utilities consideration in fault level management, extensive research and development on ways of reducing the initial capital cost are still required. Further analysis however, revealed that the financial viability of a solution is significantly dependent on the cost of energy. When one compares the life cycle costs of the various technologies considered in the South African context (Figure 4) to those costs if one assumed the energy cost to be five times more expensive (Figure 5), it is evident that the SFCL becomes much more viable option financially when the cost of energy is higher. It is generally accepted that the cost of energy in South Africa is significantly cheaper than that found in Europe, which could explain the justification for utilization of an SFCL in some European countries.

Another contributing factor which would also favour the SFCL in some European countries is the lack of carbon reduction subsidies in South Africa. The earlier quoted purchase of two SFCLs for the Birmingham network [15] is financed significantly (EUR 20 Million) from the 'Low Carbon Networks Fund' which is an initiative for reducing carbon dioxide emissions.

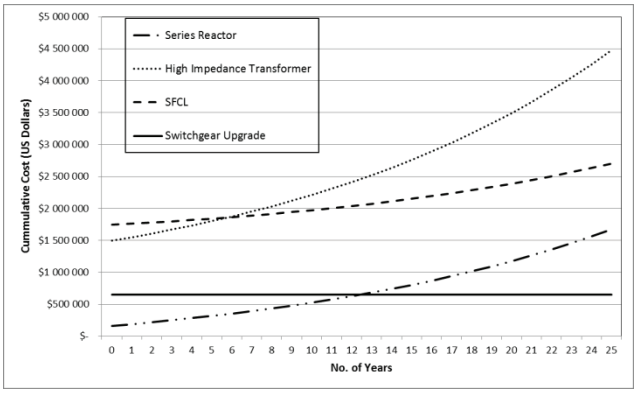


Figure 5: Accumulated cost of fault management options when assuming the cost of energy to be 5 times greater than the present South African case. (Based on an exchange rate of R 14.21/ Euro and R 10.60/ $)

As Figure 5 illustrates, variation in the cost of energy has a significant impact on the lifecycle costs of the options considered. Intersection points clearly show after how many years options would a higher capital investment cost become more cost effective when compared to solutions that have a lower capital investment but higher energy requirement.

Figure 6 compares the lifecycle cost of a switchgear upgrade with a series reactor utilizing three different energy prices (the present, double and five times the South African energy price). It shows the circuit breaker replacement option becoming increasingly preferable as an option as the cost of energy increases.

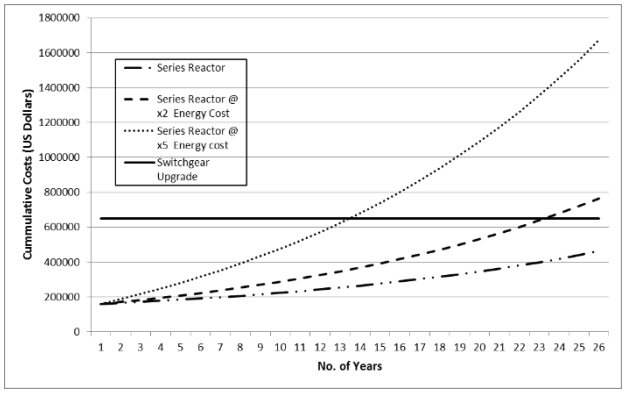


Figure 6: Accumulated cost of the switchgear upgrade option when compared to the accumulated cost of a series reactor at varying costs of energy. (Based on an exchange rate of R 14.21/ Euro and R 10.60/ $)

5. Conclusion

This paper shows that even small (< 5 MW) distributed generation projects have the potential to result in circuit breaker exceedance at a substation that would need to be addressed for operational and safety concerns. Of the fault level management technologies investigated for this case study, it was shown that the lowest 'energy cost' solution was not necessarily the most cost effective over a 25 year life cycle. There are many criteria to be considered when selecting an appropriate fault level management solution and these are, but are not limited to;

- Space constraints
- Cost of energy
- Capital cost of equipment
- Age of equipment, and
- Carbon emission reduction targets

An important note to consider is that the SFCL is an emerging technology and therefore does not benefit as yet from the advantages of 'economies of scale'. The components of SFCLs are also continuously evolving at a rapid pace (eg. more efficient cryo-coolers, a reduction in the cost of HTS tape), which would result in a more competitive option in the future. Furthermore, utilization of a superconducting fault current limiter may address other power system related concerns e.g. the reduction of transformer inrush current [16] or a network voltage unbalance improvement [17]. However, technical challenges associated with emerging technologies need to also be taken into consideration e.g. specialized maintenance.

The cost of electricity used was found to have a significant impact on the life cycle costs for the various options considered. As the cost of electricity in South Africa is comparatively low when compared to other utilities around the world, SFCLs need to therefore significantly reduce their capital cost before it can become a viable fault level management option in South Africa. However continued electricity tariff hikes may significantly alter that variable, making it financially feasible to invest in devices that utilize less energy to undertake the same function.

It would not be feasible for a power utility to adopt a single strategy to address the challenges of increasing fault levels. One should rather evaluate the various options for individual substations on a case by case basis as there are factors other than just capital cost that one needs to consider before deciding on a solution. As an example, a substation that is space constrained may need to employ a high impedance transformer to lower fault levels even though research indicates that it is the most expensive option from a lifecycle cost.

6. REFERENCES

[1] J. R. Prigmore, J.A. Mendoza, G.G. Karady, "Comparison of Four Different Types of Ferromagnetic Materials for Fault Current Limiter Applications," *IEEE Trans.Power Delivery*, Vol. 28 No. 3, July 2013, pp 1491 – 1498.

[2] B. W. Lee, J. Sim, K. B. Park, and I. S. Oh, "Practical Application Issues of Superconducting Fault Current Limiters for Electric Power Systems," *IEEE Trans. Appl. Supercond.* , Vol. 18, No. 2, June 2008, pp 620 – 623.

[3] C.J. Mozina, "Impact of Smart Grid and Green Power Generation on Distribution Systems", *IEEE Trans Ind. Applicat.*, Vol 49, Issue 3, 2011, 06175625.

[4] Y.M. Atwa *et al.,* Optimal renewable resources mix for distribution system energy loss minimization", *IEEE Trans.Power Syst.*, Vol 25, No. 1, Feb 2010, pp 360 – 370.

[5] M. Noe, A. Hobl, P Tixador, L Martini, and B Dutoit, "Conceptual Design of a 24 kV, 1 kA Resistive Superconducting Fault Current Limiter," *IEEE Trans. Appl. Supercond.* **23** 5600304.

[6] M. J. Kim *et al.,* "The application of fault current limiter at Icheon substation in Korea," *1st International Conference on Electric Power Equipment – Switching Technology (ICEPE-ST)*, 2011, pp 362 -365.

[7] M.S. El Moursi, R Hegazy, " Novel technique for reducing the high fault currents and enhancing the security of ADWEA power system", *IEEE Trans. Power Syst.*, Vol. 28, No. 1, Feb 2013, pp 140 – 148.

[8] http://integratedreport.eskom.co.za/pdf/full-integrated.pdf (accessed on 02 July 2015)

[9] NERSA News, Official Newsletter of the National Energy Regulator of South Africa, Vol VI, Edition II, 2011.

[10] RSA Grid Code Secretariat (2014). Distribution Network Code Version 6.0, July 2014.

[11] M. Mitolo, P.E. Sutherland, R. Natarajan, "Effects of high fault currents on ground grid design", IEEE Trans Ind Appl., Vol. 46, Issue 3, 04025469.

[12] G. Didier, J. Leveque, A. Rezzoug, " A novel approach to determine the optimal location of SFCL in electric power grid to improve power system stability", *IEEE Trans. on Power Syst.*, Vol. 28, No. 2, May 2013, pp 978 – 984.

[13] M. Fotuhi-Firuzabad, F. Aminifar, and I Rahmati, " Reliability study of HV substations equipped with the fault current limiter", *IEEE Trans. Power Delivery,* Vol. 27, No. 2, April 2012, pp 610 – 617.

[14] R. Kelly, "Specification for 11 kV and 22 kV withdrawable pattern air insulated Indoor primary switchgear, Eskom Doc No. 34-1157, 2012.

[15] A. Afanoukoe, "Nexan's supplies two super-conducting fault current limiters for permanent use on Birmingham's distribution network," Nexans Press Release, Paris, March 31 2014.

[16] H. Seo *et al.*, "Superconducting Fault Current Limiter Application for Reduction of the Transformer Inrush Current: A Decision Scheme of the Optimal Insertion Resistance," *IEEE Trans. Appl. Supercond.* Vol. 20, No. 4, Aug 2010, pp 2255 – 2264.

[17] J. Huh *et al.,* "Study on Voltage Unbalance Improvement Using SFCL in Power Feed network with Electric Railway System," *IEEE Trans. Appl. Supercond.* Vol. 23, No. 3, Jun 2013, 3601004

SAIEE AFRICA RESEARCH JOURNAL – NOTES FOR AUTHORS

This journal publishes research, survey and expository contributions in the field of electrical, electronics, computer, information and communications engineering. Articles may be of a theoretical or applied nature, must be novel and must not have been published elsewhere.

Nature of Articles

Two types of articles may be submitted:

- Papers: Presentation of significant research and development and/or novel applications in electrical, electronic, computer, information or communications engineering.
- Research and Development Notes: Brief technical contributions, technical comments on published papers or on electrical engineering topics.

All contributions are reviewed with the aid of appropriate reviewers. A slightly simplified review procedure is used in the case of Research and Development Notes, to minimize publication delays. No maximum length for a paper is prescribed. However, authors should keep in mind that a significant factor in the review of the manuscript will be its length relative to its content and clarity of writing. Membership of the SAIEE is not required.

Process for initial submission of manuscript

Preferred submission is by e-mail in electronic MS Word and PDF formats. PDF format files should be 'press optimised' and include all embedded fonts, diagrams etc. All diagrams to be in black and white (not colour). For printed submissions contact the Managing Editor. Submissions should be made to:

The Managing Editor, SAIEE Africa Research Journal,
PO Box 751253, Gardenview 2047, South Africa.
E-mail: researchjournal@saiee.org.za

These submissions will be used in the review process. Receipt will be acknowledged by the Editor-in-Chief and subsequently by the assigned Specialist Editor, who will further handle the paper and all correspondence pertaining to it. Once accepted for publication, you will be notified of acceptance and of any alterations necessary. You will then be requested to prepare and submit the final script. The initial paper should be structured as follows:

- TITLE in capitals, not underlined.
- Author name(s): First name(s) or initials, surname (without academic title or preposition 'by')
- Abstract, in single spacing, not exceeding 20 lines.
- List of references (references to published literature should be cited in the text using Arabic numerals in square brackets and arranged in numerical order in the List of References).
- Author(s) affiliation and postal address(es), and email address(es).
- Footnotes, if unavoidable, should be typed in single spacing.
- Authors must refer to the website: http: //www.saiee.org.za/arj where detailed guidelines, including templates, are provided.

Format of the final manuscript

The final manuscript will be produced in a 'direct to plate' process. The assigned Specialist Editor will provide you with instructions for preparation of the final manuscript and required format, to be submitted directly to:
The Managing Editor, SAIEE Africa Research Journal, PO Box 751253, Gardenview 2047, South Africa.
E-mail: researchjournal@saiee.org.za

Page charges

A page charge of R200 per page will be charged to offset some of the expenses incurred in publishing the work. Detailed instructions will be sent to you once your manuscript has been accepted for publication.

Additional copies

An additional copy of the issue in which articles appear, will be provided free of charge to authors.
If the page charge is honoured the authors will also receive 10 free reprints without covers.

Copyright

South African Institute for Electrical Engineers (SAIEE)
PO Box 751253, Gardenview, 2047, South Africa
Tel: 27 11 487 3003 | Fax: 27 11 487 3002
E-mail: researchjournal@saiee.org.za | Website: www.saiee.org.za