

SOFTWARE AIDED DESIGN OF A CMOS BASED POWER AMPLIFIER DEPLOYING A PASSIVE INDUCTOR.

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Abstract: This paper presents the design methodology of an integrated power amplifier, and coins the methodology as a software routine: for a given set of power amplifier specifications and CMOS process parameters, the routine computes the passive component values for a Class-E based power amplifier. The routine includes the matching network for standard impedance loads. The program also provides its user with a spiral inductor calculator, which can be used to determine inductance and parasitic values for an integrated square planar spiral inductor. The same tool has the ability to extract a Simulation Program With Integrated Circuit Emphasis netlist of inductor geometry, which can be used in the post-layout simulations of the power amplifier. Operation of the program was demonstrated by simulations in Austria Microsystems 0.35 μm single-supply process for a 10 dBm, 2.4 GHz power amplifier design.

Key words: Power amplifier, spiral inductor, Class-E amplifier, impedance matching, SPICE netlist.

1. INTRODUCTION

Power amplifiers (PAs) remain a bottleneck in the full integration of wireless transceivers, especially if integration is done in pure Silicon CMOS processes. For this reason, most commercial solutions for wireless LAN (WLAN) use an external PA to drive an antenna. This external device is usually fabricated in technologies superior to Silicon CMOS, such as Silicon-Germanium, Gallium-Arsenide, Indium-Phosphate or Gallium-Nitride processes. Additionally, the integrated PA disturbs analogue signals if it is fabricated on the same IC, and its performance is inferior compared to the external PA devices.

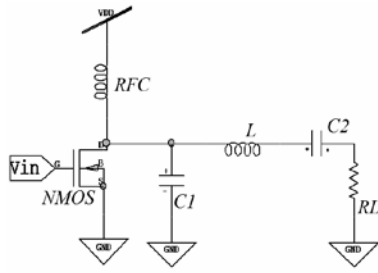
Nevertheless, it is not always possible to separate a PA from the rest of the system, so the designers often have to be satisfied with a simple PA design in a pure Silicon CMOS process.

In many radio frequency (RF) modulation schemes, such as the Direct Sequence Spread Spectrum (DSSS) technique, it is necessary to design several PAs in order to ensure operation in different channels of the same band. For example, for a system based on DSSS [1], transmission is possible over a number of channels in the Industrial, Scientific and Medical (ISM) band; their centre frequencies ranging from 2.4000 GHz to 2.4835 GHz. If the design procedure is not aided by a computer program, designing of all PAs for all channels can be quite time consuming.

Irrespective of the configuration of the PA used in the design, in addition to active components (MOSFET transistors), a number of passive components (inductors

and capacitors) should be included. In SPICE (Simulation Program With Integrated Circuit Emphasis) simulations at schematic design level this does not present a problem, because ideal capacitors and inductors can be used. However, translation of the design onto layout level (where layout refers to actual drawing of components for a silicon wafer) becomes more intricate. Each capacitor and inductor must be designed separately using different silicon and/or metal layers. After completing the design of these components, their netlists are extracted, and ideal components from the schematic level are then replaced with non-ideal layout-drawn components.

In the case of a capacitor, the layout tool is provided with built-in procedures for its SPICE netlist extraction, and the actual capacitance of drawn components can be checked. If necessary, this value can be fine-tuned by slightly modifying the geometry of the component. Unfortunately, in more affordable electronic design automation (EDA) software, for instance Tanner Tools, this does not apply to inductors. The built-in SPICE netlist extractor "sees" the inductor as simply a long piece of metal or wire (which short-circuits the nodes placed at the two ends of an inductor), thus making the extracted netlist incorrect. In order to perform post-layout simulations, this can be rectified by inserting "ideal" inductors between the short-circuited nodes, which in turn leads to incorrect simulation results. Such an approach becomes particularly inappropriate in the design of PAs, due to the fact that even small differences between actual and designed values of inductance can strongly affect the centre frequency or the gain of the amplifier. Often these mismatches can only be seen after the fabrication of the chip is completed.



(a) Schematic presentation of a PA [3]

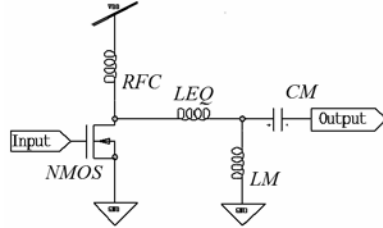
(b) PA with components L_{EQ} , C_M and L_M calculated by the PA design program

Figure 1: Designed CMOS power amplifier

In this paper, a computer program is presented to simplify the design process of integrated PAs and inductors associated with them, especially in cases where time is at stake. A number of parameters, such as centre frequency, required output power and the power supply voltage are taken as inputs to this program. Values of the passive components are then calculated and optimized. The program also performs impedance matching for standard antenna impedances (50 Ω).

The program offers an option to calculate inductance and parasitic values for given spiral inductor geometries in order to aid the designer in the layout design. Finally, the netlist for such inductor geometry can be extracted. The designer can then place this netlist directly into the netlist of the global system extracted by SPICE to adequately compensate for the abovementioned short-circuit problem.

2. POWER AMPLIFIER DESIGN EQUATIONS

A number of simple PA output stages are available in modern electronics. Some of these stages, such as Class A, Class AB or Class C are commonly used in power electronics. For RF ICs, Class-E and Class-F stages are more suited [2].

The PA program presented here computes component values for the Class-E stage, as shown in Figure 1(a) [2]. This configuration is powered from a single power supply, V_{DD} .

If the required output power is labelled as P_O , the optimum load resistance can be calculated as [3]:

$$R_L = 0.577 \frac{V_{DD}^2}{P_O} \quad (1)$$

Furthermore, if Q is defined as quality factor (Q-factor) of the PA by letting

$$Q = \omega_0 / BW \quad (2)$$

where:

BW = transmission bandwidth

ω_0 = centre transmission frequency in rad/s

then values for three passive components from Figure 1(a) (one inductor and two capacitors) can be calculated as follows:

$$C_1 \approx \frac{1}{5.447 \omega_0 R_L} \quad (3)$$

$$L = \frac{Q R_L}{\omega_0} \quad (4)$$

and:

$$C_2 \approx C_1 \frac{5.447}{Q} \left(1 + \frac{1.42}{Q - 2.08} \right) \quad (5)$$

In most schematic designs, capacitor C_1 is omitted, because this value is on the same order as the value of parasitic drain-to-source capacitance of the transistor. In general, the parasitic effects of the transistor are not taken into account by the PA design program, as they are process specific. It is assumed that the designer will be responsible for further fine-tuning a PA for its correct operation.

Equations 3, 4 and 5 are sufficient for the design of a PA if it is driving the antenna with impedance calculated in Equation 1. However, this value of R_L is a non-standard load impedance, so impedance matching to the actual load has to be done. The PA program performs this matching by introducing a high pass reactive-L-type matching network, with an inductor (L_M) connected between the output of the PA and ground, and a capacitor (C_M) connected between the output of the PA and the load. This configuration is chosen specifically so that capacitor C_M can at the same time serve as decoupling capacitor for the load. Since both output impedance of the PA and the impedance of load are real values, a complex matching procedure, traditionally performed on Smith charts, can be simplified to evaluating the following two real formulas [4]:

$$L_M = \frac{1}{\omega_0} \left(\frac{R_O^2 R_M}{R_O - R_M} \right)^{1/2} \quad (6)$$

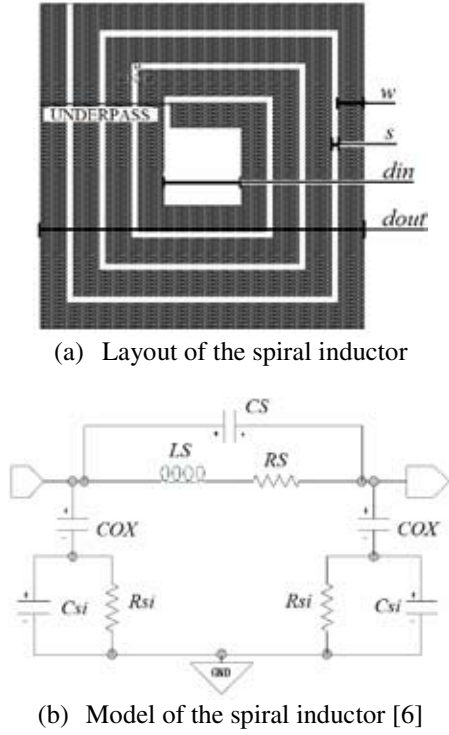


Figure 2: Layout and model of the spiral inductor

and:

$$C_M = \frac{1}{\omega_0} \left(\frac{R_o^2 + (\omega_0 L_M)^2}{R_o^2 (\omega_0 L_M)} \right) \quad (7)$$

Finally, due to the very high value of the calculated Q-factor, the value of the calculated inductor L is higher than the practical value, whilst the value of the capacitor C_2 is lower than the practical value. These two components appear in series, and more practical values can be obtained applying the procedure described in [5]. If Z_L is the impedance of the inductor L and Z_{C2} the impedance of capacitor C_2 , then the equivalent impedance is:

$$Z_{EQ} = Z_L + Z_{C2} \quad (8)$$

This results in a single inductor of value (L_{EQ}) practical for microelectronic integration.

Figure 1(b) shows the final PA circuit, with all components calculated using the PA design program. This program does not suggest the transistor aspect ratio (W/L). However, to ensure that the output stage has voltage gain larger than 1, this ratio should be kept as high as possible. For the Austria Microsystems (AMS) CMOS 0.35 μm process, this value was chosen to be the highest allowed, (200 μm)/(0.35 μm).

3. SPIRAL INDUCTOR DESIGN EQUATIONS

Demand for low-cost ICs has generated high interest in integrated passive components. Whilst capacitor and resistor implementations are easy to model, as discussed before, considerable effort has been invested in the design of integrated inductors [6]. Two practical options are bond wires and planar spiral inductors. Bond wires allow for high Q-factor of the inductor to be achieved, where Q-factor is defined as $Q = \text{Im}(Z)/\text{Re}(Z)$ and Z is the impedance of the inductor, which is different from the PA Q-factor described in Section 2. However, the range of possible inductances for bond wire inductors is limited, leaving spiral inductors as the only other feasible option for integration. Although the Q-factor of the spiral inductor is lower than the Q-factor of the bond wire inductor, its inductance is well-defined over a broader range of process variations.

A number of spiral inductor configurations are commonly used, amongst them square, hexagonal, octagonal and circular. Figure 2(a) shows the layout of a square inductor. Because of the ease of its layout, the PA design program suggests this configuration for implementing inductors for the designed PA.

Although the idea behind the process of designing a spiral inductor is to get as close as possible to the desired inductance values, some parasitic effects cannot be avoided. For the purpose of expanding the PA design program, the inductance value, and not the Q-factor, is considered important for the design. Parasitic values are still calculated, and included in the netlist. Figure 2(b) shows the circuit model for the spiral inductor.

A spiral inductor is fully specified by the number of turns (n), the turn width (w) and two of the following: inner, outer or average diameter (d_{in} , d_{out} or $d_{avg} = (d_{in} + d_{out})/2$), as shown in Figure 2(a). The spacing between the turns (s) can be calculated from the other parameters.

3.1 Inductance (L_S)

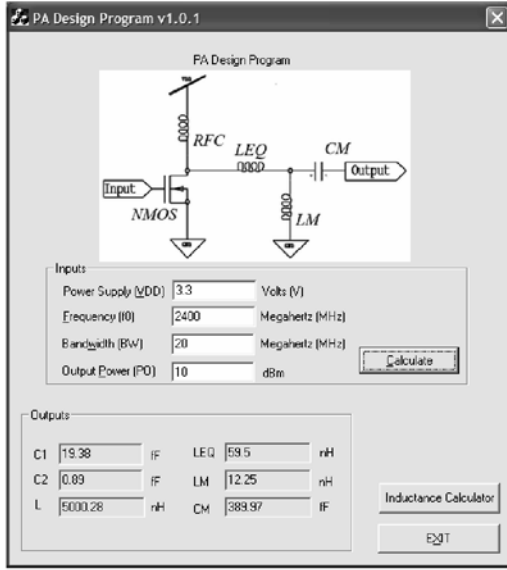
Inductance of the square spiral inductor is calculated by means of a data fitted monomial expression [6][7] (with inductor dimensions in micrometer):

$$L_S = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \text{ (nH)} \quad (9)$$

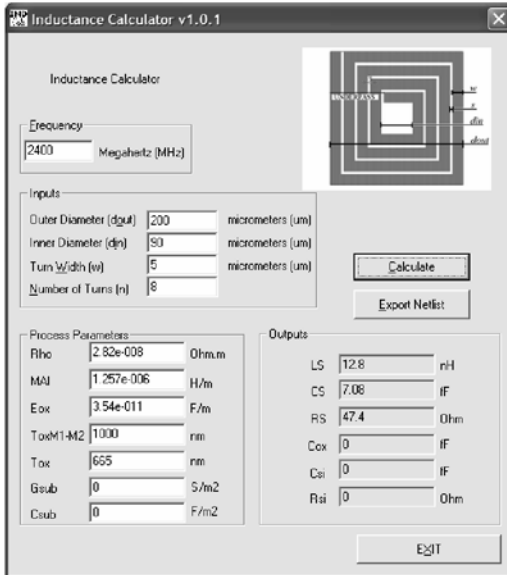
Above, the coefficients β , α_1 , α_2 , α_3 , α_4 and α_5 are obtained numerically and presented in Table I [6]. This expression yields the typical error of less than 3%.

Table I: Coefficients for square spiral inductor inductance calculation

β	$\alpha_1 (d_{out})$	$\alpha_2 (w)$	$\alpha_3 (d_{avg})$	$\alpha_4 (n)$	$\alpha_5 (s)$
$1.62 \cdot 10^{-3}$	-1.21	-0.147	2.40	1.78	-0.030



(a) User screen of the PA design program



(b) User screen of the inductance calculator

Figure 3: User screens and of PA design program and inductance calculator.

3.2 Parasitic resistance (R_s)

The parasitic resistance is dependent on the frequency of operation. At DC, this value is mostly dependent on sheet resistance of the material of which the wire is made. At high frequencies, this is overshadowed by the resistance that arises due to formation of eddy currents. It depends on the resistivity of the metal layer in which the inductor is laid out (ρ), total length of all inductor segments (l), width of the inductor (w) and its effective thickness (t_{eff}) [8]:

$$R_s = \frac{\rho l}{wt_{eff}} \quad (10)$$

Effective thickness, t_{eff} , is dependent on the actual thickness of the metal layer, t :

$$t_{eff} = \delta(1 - e^{-t/\delta}) \quad (11)$$

where δ is frequency-dependent skin depth:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \quad (12)$$

Parameter μ is the permeability of the metal layer.

3.3 Parasitic capacitance (C_s)

The parasitic capacitance is the sum of all overlap capacitances created between the spiral and the underpass. If the underpass has the same width as the spiral, then the capacitance is equal to [8]:

$$C_s = nw^2 \frac{\epsilon_{ox}}{t_{oxM1-M2}} \quad (13)$$

where:

$t_{oxM1-M2}$ = oxide thickness between the spiral and the underpass

ϵ_{ox} = dielectric constant of the oxide layer between the two metals.

3.4 Substrate parasitic quantities (C_{ox} , C_{Si} and R_{Si})

Substrate parasitic quantities are approximately proportional to the area occupied by the inductor and can be estimated as [8]:

$$C_{ox} = \frac{1}{2} lw \frac{\epsilon_{ox}}{t_{ox}} \quad (14)$$

$$C_{Si} = \frac{1}{2} lw C_{sub} \quad (15)$$

and:

$$R_{Si} = \frac{2}{lw G_{sub}} \quad (16)$$

where:

C_{sub} = capacitance per unit area for the silicon substrate

G_{sub} = conductance per unit area for the silicon substrate

ϵ_{ox} = dielectric constant of the oxide layer between the inductor and the substrate

t_{ox} = thickness of the oxide layer.

These expressions are sufficient for modelling the spiral inductors for the requirements of the PA design program [7].

4. THE PROGRAM

The PA design program was written in Visual C++.

4.1 Power amplifier design part of the program

The primary screen of the PA design program is shown in Figure 3(a). This screen is used to calculate values of the PA passive components. The user inputs the power supply voltage (V_{DD}) in volts, required output power (P_O) in dBm, centre frequency of the channel over which the amplifier operates (f_0) in MHz and allowed bandwidth (BW) in MHz. Values of capacitors C_1 , C_2 and inductors L and L_{EQ} , together with matching parameters C_M and L_M are then computed and displayed. Although L_{EQ} , C_M and L_M are sufficient for the complete simulation using ideal passive components, the non-simplified values C_1 , C_2 and L are available for experimentation by the user.

4.2 Spiral inductor design part of the program

This part performs the secondary function of the program. In order to design real spiral inductors, the user is allowed to specify the geometry of the square inductor and see the resulting inductance. Figure 3(b) shows the user screen of the inductance calculator. The user needs to input the geometry of the inductor, namely the outer diameter (d_{out}), inner diameter (d_{in}), width of one turn (w), all in μm , and the number of turns (n). Process-specific values for calculating parasitic quantities need not be specified, as default parameters are used (for the AMS 0.35 μm process). If necessary, they can be replaced with specific technology parameters. Specifically, the program uses resistivity and permeability values for aluminium wires, as shown in Table II, as well as frequency specified by the user in the primary screen, as defaults for calculating the parasitic resistance. For the calculation of other parasitic quantities, common process values are used as shown in Table II. Finally, the user is allowed to specify G_{sub} and C_{sub} for calculations of C_{si} and R_{si} . If these parameters are omitted, calculations of parasitic values C_{ox} , C_{si} and R_{si} are not performed.

Table II: Parameters for spiral inductor parasitics calculation

ρ_{Al} [$\Omega\cdot\text{m}$]	μ_{Al} [H/m]	ε_{ox} [F/m]	$t_{oxM1-M2}$ [nm]	t_{ox} [nm]
$2.82\cdot 10^{-8}$	$1.4\pi\cdot 10^{-7}$	$4.885\cdot 10^{-12}$	1000	665

Optimization of the spiral inductor is performed by modifying the dimensions or trace width of the inductor. In general, the inductance can be increased by decreasing the trace width and increasing the number of turns, which, in turn, increases the parasitic resistance R_S and subsequently decreases the Q-factor of the inductor.

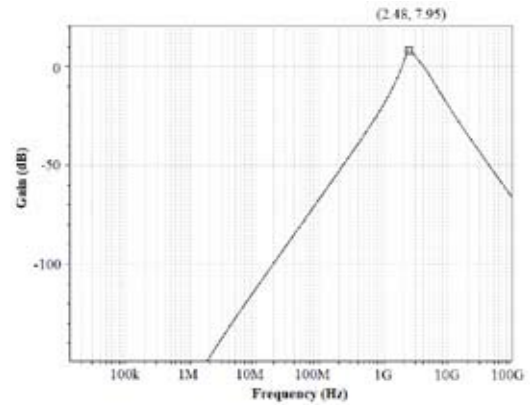
4.3 Spiral inductor netlist extraction

After a few geometry iterations, a correct inductor value can be generated, and a SPICE netlist exported (Figure 3(b)). An example of such a netlist is shown in Figure 4.

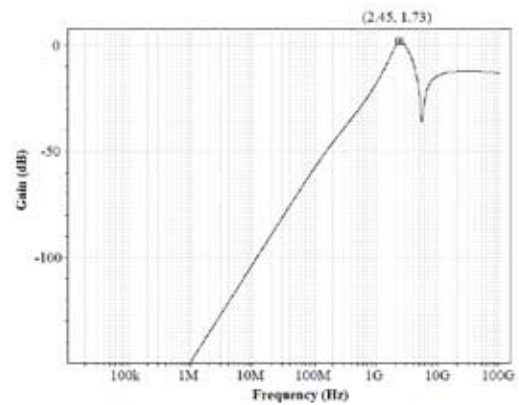
```
*Include the following code before Main Circuit
*SUBCKT gen. by Ind. Calc. v1.0.0
.SUBCKT Inductor_Model L1 L2 GND
CS L1 L2 1fF
Csi1 N2 GND 1fF
Csi2 N3 GND 1fF
Cox1 L1 N2 1fF
Cox2 L2 N3 1fF
LS N4 L1 1n
Rsi1 N2 GND 10
Rsi2 N3 GND 10
RS N4 L2 10
.ENDS

*Include the following line in Main Circuit
*instead of your ideal inductor
*and replacing nodes L1 and L2 with original
ones
XInductor_Model_1 L1 L2 IndModLEQ
```

Figure 4: Example of SPICE netlist of spiral inductor model.



(a) Bode plot of the gain of PA employing ideal inductors



(b) Bode plot of the gain of PA employing a spiral inductor designed per Figure 3

Figure 5: Simulation Bode plots

5. SIMULATION RESULTS

SPICE simulations of the extracted netlists were performed in Silicon CMOS 0.35 μm process from AMS. This process was used to verify operation of a PA, employing both ideal inductors (infinite Q-factor) and spiral inductors (finite Q-factor). This process is powered from a typical single power supply of 3.3 V.

```

...
C1 N3 N2 390fF
L2 VDD N5 50n *RFC
L3 N5 N4 59.50n *LEQ
L4 N3 GND 12.25n *LM
XPowerSupply_1 GND MST_RST VDD PowerSupply
R5 N2 GND 50
XRFNMOS7 N5 N9 GND GND MODNRF W=200u L=0.35u
NG=40
v8 N8 GND sin(0.9 1 2.4E9 0 0 0)
v9 N9 N8 AC 0.2 0
...

```

(a) Snippet of the netlist of a PA with ideal inductors

```

...
*Include the following code before Main Circuit
*SUBCKT gen. by Ind. Calc. v1.0.0
.SUBCKT IndModLM L1 L2
CS L1 L2 7.08fF
LS N1 L1 12.8n
RS N1 L2 47.40
*Ignoring Csub,Gsub
.ENDS

*Include the following code before Main Circuit
*SUBCKT gen. by Ind. Calc. v1.0.0
.SUBCKT IndModLEQ L1 L2
CS L1 L2 14.16fF
LS N1 L1 59.09n
RS N1 L2 130.8
*Ignoring Csub,Gsub
.ENDS

...
C1 N3 N2 390fF
*Include the following line in Main Circuit
*instead of your ideal inductor
*and replacing nodes L1 and L2 with original
ones
XIndModLEQ_1 N5 N4 IndModLEQ
*Include the following line in Main Circuit
*instead of your ideal inductor
*and replacing nodes L1 and L2 with original
ones
XIndModLM_1 GND N3 IndModLM
L2 VDD N5 50n *RFC
XPowerSupply_1 GND MST_RST VDD PowerSupply
R5 N2 GND 50
XRFNMOS4 N5 N9 GND GND MODNRF W=200u L=0.35u
NG=40
V8 N8 GND sin(0.9 1 2.4E9 0 0 0)
V9 N9 N8 AC 0.2 0
...

```

(b) Snippet of the netlist of a PA with ideal inductors replaced with inductor netlists generated by inductance calculator part of the program

Figure 6: Netlist snippets

In the simulation example, it was assumed that power amplification was done for an analogue signal operating in ISM band, with centre frequency of 2.4 GHz and channel width of 20 MHz. Although for the schemes such as DSSS, centre frequencies are just above 2.4 GHz and channel widths are 22 MHz, these parameters are sufficient for the simulations of interest. Further, the required output power of the stage was assumed at 10 dBm. Figure 5(a) shows the Bode plot of the PA gain, using a 50 Ω antenna for a SPICE simulation performed on a netlist (with “ideal” inductors). The snippet of this netlist is shown in Figure 6(a). Figure 5(b) shows the same plot, but with ideal inductors in the netlist of

Figure 6(a) replaced by spiral inductors, designed by the secondary function of the PA design program. This presents an emulation of the post-layout simulation. The snippet of this netlist is shown in Figure 6(b). Table III presents the summary of technical parameters, PA component values, inductor geometry parameters, as well as measured parameters for the simulated circuits.

Table III: Inputs, outputs and parameters used in PA simulations

Technical Parameters		Design Parameters (Spiral Inductor)		
Parameter	Value	Parameter	Value (L_{EQ})	Value (L_M)
f_0 [GHz]	2.4	d_{out} [μ m]	300	200
BW [MHz]	20	d_{in} [μ m]	100	90
P_{out} [dBm]	10	w [μ m]	5	5
V_{DD} [V]	3.3	n	16	8
Calculated Component Values (PA)		Calculated Inductance and Parasitics (Spiral Inductor)		
Parameter	Value	Parameter	Value (L_{EQ})	Value (L_M)
C_1 [fF]	19.38	L_S [nH]	59.09	12.8
C_2 [fF]	0.89	R_S [Ω]	130.81	47.40
L [μ H]	5	C_S [fF]	14.16	7.08
L_{EQ} [nH]	59.5	C_{ox} [fF]	Ignored	Ignored
L_M [nH]	12.25	C_{st} [μ F]	Ignored	Ignored
C_M [fF]	389.97			
Measured Parameters (Q_i ?)		Measured Parameters (Q_i < ?)		
Parameter	Value	Parameter	Value	
f_0 [GHz]	2.48	f_0 [GHz]	2.45	
Gain [dB]	7.95	Gain [dB]	1.73	
P_{out} [dBm]	~ 9	P_{out} [dBm]	~ 4	

6. DISCUSSION

As it is evident from Table III, the centre frequency of the waveform in Figure 5(a) is higher than anticipated by calculations (Figure 3(b)). This effect is due to the parasitic capacitance of the transistor, and the lack of physical capacitor, C_1 . The software routine developed in this paper aims to produce a first approximation for the design only, therefore this higher value of the centre frequency was considered acceptable. A further fine tuning of the values of other passive components, namely L_{EQ} , L_M and C_M can assist to obtain a more exact centre frequency. The output power (P_O) is close to the value designed (Figure 3(a)). A similar response is obtained after introducing the spiral inductors, as seen in Figure 5(b). However, a lower gain and lower output power are observed at the peak frequency, which can be attributed to the low inductor Q-factor. The zero at approximately 5 GHz is due to the capacitive effect of C_S of the spiral inductor L_{EQ} , whilst other parasitic elements do not have noticeable influence on the shape of the gain plot at frequencies of interest. It should also be noted that this Bode plot is accurate only for frequencies close to the design frequency, i.e. 2.4 GHz, because of the frequency dependency on the parasitic resistance, R_S . In general, it is evident that simulation results with parameters calculated by the PA design program shows good agreement with the PA's theoretical behaviour.

7. CONCLUSION

In this paper, a PA design program for ICs has been presented. The program can be used for three main purposes. Firstly, to determine parameters for Class-E PA output stages based on the set of equations presented in [2] and [3]. It also performs otherwise tedious impedance matching to standard impedance loads, such as 50 Ω , whilst providing suggestions on how to simplify some component values.

Secondly, the program can be used to calculate inductance and parasitic values for the square planar spiral inductor based on equations from [6] and [8]. Although the user is allowed to modify geometry to improve the quality factor of such an inductor, the main concern of this part of the program is to allow the user to get as close as possible to the required inductance value.

Thirdly, the program can be used to export a SPICE netlist of spiral inductor geometry to be used in post-layout simulations. This is considered essential, since most SPICE simulators interpret an integrated spiral inductor as a long stretch of wire (or a resistor).

To verify the parameters computed by the program, simulations, using the 0.35 μm process, were performed for designing a 10 dBm PA operating in ISM band with centre frequency of about 2.4 GHz. Two separate configurations were simulated: with ideal inductors and by using the spiral inductor program of this paper. The two simulations compared well.

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